

# 8Gb DDR4 SDRAM

(RoHS Compliant)

**EC4S8G08A**

**EC4S8G16A**

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## 1 Ordering Information

Table 1 – 8Gb DDR4 ordering information table

Commercial Grade				
Organization	Part Number	Data Rate (Mb/s)	CL-tRCD-tRP	Package
1G x 8	EC4S8G08A-24C	DDR4-2400	17-17-17	78 Ball FBGA
	EC4S8G08A-26C	DDR4-2666	19-19-19	
	EC4S8G08A-29C	DDR4-2933	21-21-21	
	EC4S8G08A-32C	DDR4-3200	22-22-22	
512M x 16	EC4S8G16A-24C	DDR4-2400	17-17-17	96 Ball FBGA
	EC4S8G16A-26C	DDR4-2666	19-19-19	
	EC4S8G16A-29C	DDR4-2933	21-21-21	
	EC4S8G16A-32C	DDR4-3200	22-22-22	
Industrial Grade				
Organization	Part Number	Data Rate (Mb/s)	CL-tRCD-tRP	Package
1G x 8	EC4S8G08A-24I	DDR4-2400	17-17-17	78 Ball FBGA
	EC4S8G08A-26I	DDR4-2666	19-19-19	
	EC4S8G08A-29I	DDR4-2933	21-21-21	
	EC4S8G08A-32I	DDR4-3200	22-22-22	
512M x 16	EC4S8G16A-24I	DDR4-2400	17-17-17	96 Ball FBGA
	EC4S8G16A-26I	DDR4-2666	19-19-19	
	EC4S8G16A-29I	DDR4-2933	21-21-21	
	EC4S8G16A-32I	DDR4-3200	22-22-22	

## 2 DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

*The following table lists the committed specifications based on the chip verification result. The following chapters in this document describe only the chip design specifications. For details about whether the corresponding functions are available, see the table below(Table2).*

**Table 2 - Function Matrix (By ORG. V: Supported, Blank: Not supported)**

Functions	x8	x16	NOTE
Write Leveling	V	V	
Temperature controlled Refresh			Do not support
Low Power Auto Self Refresh			Do not support
Fine Granularity Refresh	V	V	MR2 A8:A6 config to be 0b000. Fixed 1X mode
Multi Purpose Register	V	V	
Data Mask	V	V	
Data Bus Inversion			Do not support
TDQS			X8 do not support TDQS feature
ZQ calibration	V	V	
DQ Vref Training	V	V	
Per DRAM Addressability	V	V	
Mode Register Readout	V	V	
CAL	V	V	
WRITE CRC	V	V	
CA Parity			Do not support
Control Gear Down Mode			
Programmable Preamble	V	V	
Maximum Power Down Mode			
Boundary Scan Mode		V	Limited functionality, referring to description of the function of ck_t and ck_c Table 3 - DDR4 SDRAM PinOut Description
Additive Latency			
3DS			
PPR		V	X8 do not support PPR feature <b>X16 Limited Application Specifications, refer to chapter 18.4 and 18.5</b>
Others			Refer to Chapter 17

**Table 4 - Function Matrix (By Speed. V: Supported, Blank: Not supported)**

Functions	DLL Off mode	DLL On mode			NOTE
	≤ 250 Mbps	1600/1866/2133 Mbps	2400Mbps	2666/3200Mbps	
Write Leveling	V	V	V	V	
Temperature controlled Refresh					
Low Power Auto Self Refresh	V	V	V	V	
Fine Granularity Refresh	V	V	V	V	
Multi Purpose Register	V	V	V	V	
Data Mask	V	V	V	V	
Data Bus Inversion					
TDQS					
ZQ calibration	V	V	V	V	
DQ Vref Training	V	V	V	V	
Per DRAM Addressability		V	V	V	
Mode Register Readout	V	V	V	V	
CAL		V	V	V	
WRITE CRC		V	V	V	
CA Parity					
Control Gear Down Mode					
Programmable Preamble (= 2tCK)			V	V	
Maximum Power Down Mode					
Boundary Scan Mode		V	V	V	
3DS					
Others	Refer to Chapter 18				

## 3 Operating Frequency

Table 5 - 8Gb DDR4 Speed bins

Speed	DDR4-32	DDR4-293	DDR4-266	DDR4 -	DDR4 –	DDR4 -	DDR4 -
	00	3	6	2400	2133	1866	1600
	22-22-22	21-21-21	19-19-19	17-17-17	15-15-15	13-13-13	11-11-11
tCK(ns)	0.625	0.682	0.75	0.833	0.937	1.071	1.25
CAS Latency(nCK)	22	21	19	17	15	13	11
tRCD(ns)	13.75	14.32	14.25	14.16	14.06	13.92	13.75
tRP(ns)	13.75	14.32	14.25	14.16	14.06	13.92	13.75
tRAS(ns)	32	32	32	32	33	34	35
tRC(ns)	45.75	46.32	46.25	46.16	47.06	47.92	48.75

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## 4 Key Features

The transfer rates of 8Gb DDR4 can be up to 3200Mbps for general applications which requires large memory density and high bandwidth. The chip is designed to comply with the following key DDR4 SDRAM feature such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination supported and Asynchronous Reset. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fashion.

The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style.

- VDD = VDDQ = 1.2V +/- 0.06V
- VPP = 2.5V (2.375V~2.75V)
- 8Gb DDR4 SDRAM x8 = 16 Banks (4 bank group) / 8Gb DDR4 SDRAM x16 = 8 Banks (2 bank group)
- 8-bit pre-fetch
- Burst length of 8 and burst chop of 4
- Bi-directional / Differential Data-Strobe
- On Die Termination supported
- Asynchronous Reset
- ZQ calibration supported
- Programmable CAS Latency (posted CAS): 10,11,12,13,14,15,16,17,18,19,20,21,22
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency (CWL) = 12,14 (DDR4-2400);14,18 (DDR4-2666); 16, 20 (DDR4-2933 and DDR4-3200)
- Average Refresh Cycle (Tcase of 0°C ~ 95°C)
  - 7.8 μs at 0°C ~ 85°C
  - 3.9 μs at 85°C ~ 95°C
- JEDEC standard 78ball FBGA(x8), 96ball FBGA(x16)
- DLL off mode is supported
- CA parity (Command Address Parity) mode is supported
- Data Bus write CRC(Cyclic Redundancy Check) is supported
- POD (Pseudo Open Drain) interface for data input/output
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- PPR (Post Package Repair) mode is supported<sup>1</sup>
- Low Power Self Refresh mode is supported
- All of products are compliance with the RoHS directive

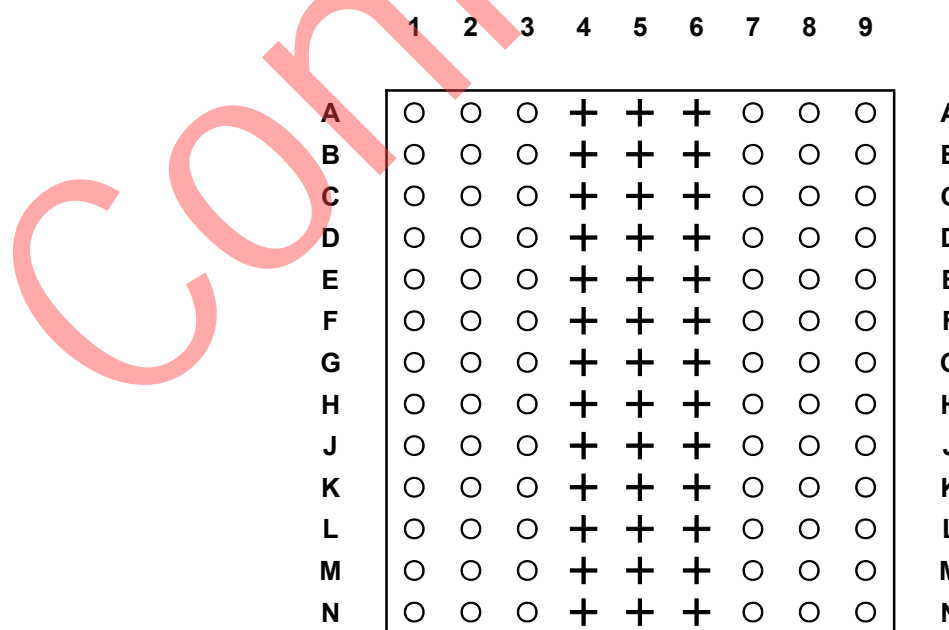
Note :

1. PPR mode is only supported in X16 configuration
2. PPR mode is supported at Precharge ALL.
3. TEN mode is only supported in X16 configuration
4. TDQS mode is NOT supported in X8 configuration

## 5 Package pinout/Mechanical Dimension & Addressing

### 5.1 DDR4 x8 Package Ball out (Top view): 78ball FBGA Package

	1	2	3	4	5	6	7	8	9
A	VDD	VSSQ	TDQS_c				DM_n, DBI_n, TDQS_t	VSSQ	VSS
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS
F	VDD	NC	ODT				CK_t	CK_c	VDD
G	VSS	NC	CKE				CS_n	NC	NC
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD
K	VSS	BA0	A4				A3	BA1	VSS
L	RESET_n	A6	A0				A1	A5	ALERT_n
M	VDD	A8	A2				A9	A7	VPP
N	VSS	A11	PAR				NC	A13	VDD

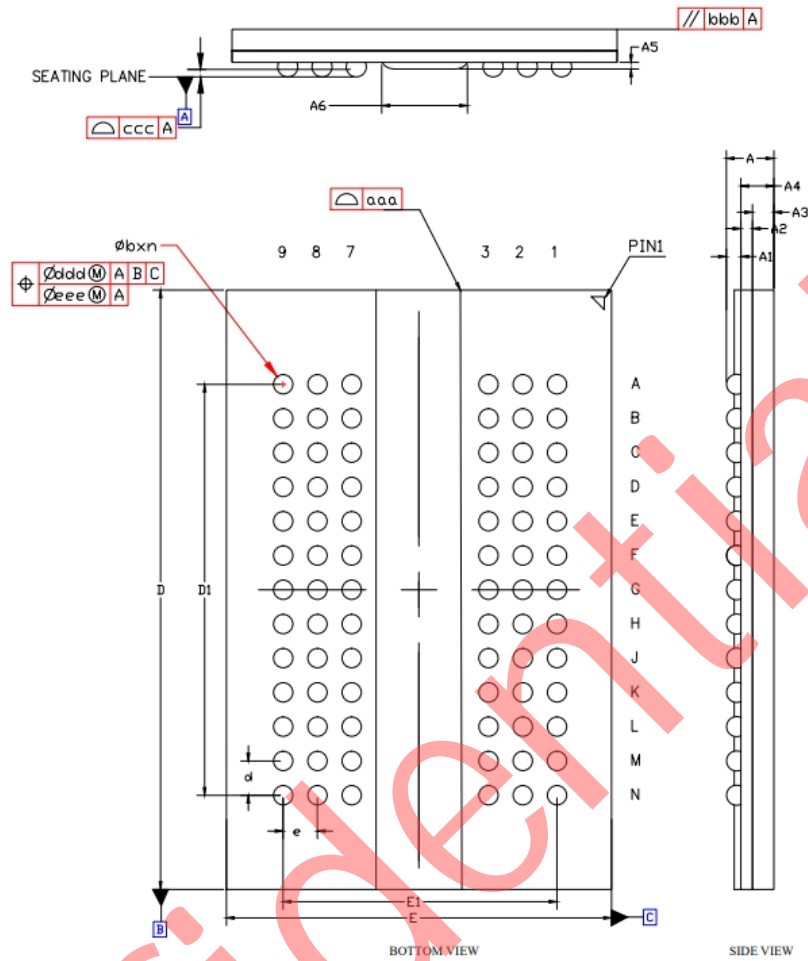


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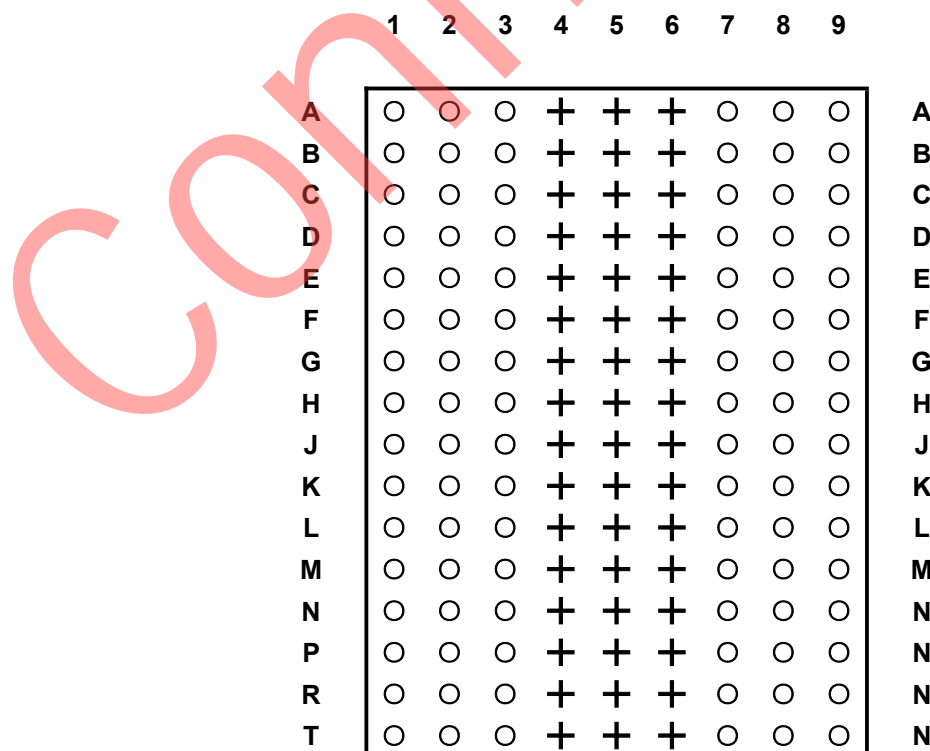
## 5.2 DDR4 x8 FBGA Package Dimension



	Symbol	Dimension in mm			Dimension in inch		
		Min	Normal	Max	Min	Normal	Max
TOTAL THICKNESS	A	---	1.12	1.20	---	0.0441	0.0472
STAND OFF	A1	0.30	0.34	0.38	0.0118	0.0134	0.0150
SUBSTRATE THICKNESS	A2	0.20	0.23	0.26	0.0079	0.0091	0.0102
MOLD THICKNESS	A3	0.52	0.55	0.58	0.0205	0.0217	0.0228
SBT+MOLD THICKNESS	A4	0.73	0.78	0.83	0.0287	0.0307	0.0327
SLOT THICKNESS	A5	0.142	0.155	0.168	0.0056	0.0061	0.0066
SLOT WIDTH	A6	1.90	2.00	2.10	0.0748	0.0787	0.0827
BALL WIDTH	phi b	0.42	0.47	0.52	0.0165	0.0185	0.0205
BALL PITCH	d	0.8			0.0315		
	e	0.8			0.0315		
BALL COUNT	n	78					
BODY SIZE	D	13.90	14.00	14.10	0.5472	0.5512	0.5551
	E	8.90	9.00	9.10	0.3504	0.3543	0.3583
EDGE BALL CENTER TO CENTER	D1	9.50	9.60	9.70	0.3740	0.3780	0.3819
	E1	6.30	6.40	6.50	0.2480	0.2520	0.2559
PKG EDGE TOLERANCE	aaa	0.10			0.0039		
MOLD FLATNESS	bbb	0.10			0.0039		
COPLANARITY	ccc	0.10			0.0039		
BALL OFFSET(PACKAGE)	ddd	0.15			0.0059		
BALL OFFSET(BALL)	eee	0.05			0.0020		
JEDEC		MO-276(REF)					

## 5.3 DDR4 x16 Package Ball out (Top view): 96ball FBGA Package

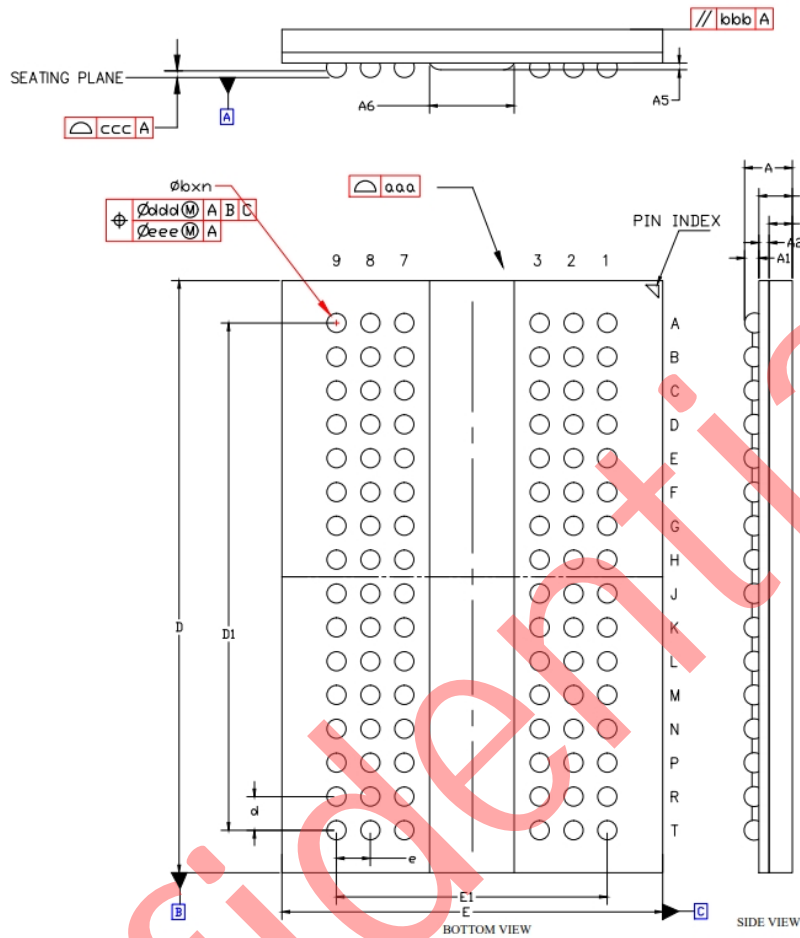
	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n/ A16	VDD	L
M	VREFCA	BG0	A10/ AP				A12/ BC_n	CAS_n/ A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T



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## 5.4 DDR4 x16 FBGA Package Dimension



	Symbol	Dimension in mm			Dimension in inch		
		Min	Normal	Max	Min	Normal	Max
TOTAL THICKNESS	A	---	1.12	1.20	---	0.0441	0.0472
STAND OFF	A1	0.30	0.34	0.38	0.0118	0.0134	0.0150
SUBSTRATE THICKNESS	A2	0.20	0.23	0.26	0.0079	0.0091	0.0102
MOLD THICKNESS	A3	0.51	0.55	0.59	0.0201	0.0217	0.0232
SBT+MOLD THICKNESS	A4	0.73	0.78	0.83	0.0287	0.0307	0.0327
SLOT THICKNESS	A5	0.142	0.155	0.168	0.0056	0.0061	0.0066
SLOT WIDTH	A6	1.90	2.00	2.10	0.0748	0.0787	0.0827
BALL WIDTH	Φb	0.42	0.47	0.52	0.0165	0.0185	0.0205
BALL PITCH	d	0.8			0.0315		
	e	0.8			0.0315		
BALL COUNT	n	96					
BODY SIZE	D	13.90	14.00	14.10	0.5472	0.5512	0.5551
	E	8.90	9.00	9.10	0.3504	0.3543	0.3583
EDGE BALL CENTER TO CENTER	D1	11.90	12.00	12.10	0.4685	0.4724	0.4764
	E1	6.30	6.40	6.50	0.2480	0.2520	0.2559
PKG EDGE TOLERANCE	aaa	0.10			0.0039		
MOLD FLATNESS	bbb	0.10			0.0039		
COPLANRITY	ccc	0.10			0.0039		
BALL OFFSET(PACKAGE)	ddd	0.15			0.0059		
BALL OFFSET(BALL)	eee	0.05			0.0020		
JEDEC		MO-276(REF)					

## 6 Pinout Description

Table 6 - DDR4 SDRAM PinOut Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c. In connectivity test mode, the clock needs to be in differential inputs and the mrs command cannot be sent.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power- Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM. RTT_NOM cannot be changed when ODT pin active;
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16, A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8

Symbol	Type	Function
<b>BG0 - BG1</b>	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
<b>BA0 - BA1</b>	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
<b>A0 - A16</b>	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands.
<b>A10 / AP</b>	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto precharge, LOW: no Autop recharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses
<b>A12 / BC_n</b>	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
<b>RESET_n</b>	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD
<b>DQ</b>	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During the mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
<b>DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c</b>	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
<b>TDQS_t, TDQS_c</b>	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.

Symbol	Type	Function
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n LOW
ALERT_n	Input / Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and not support on x4/x8 densities. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V ( 2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

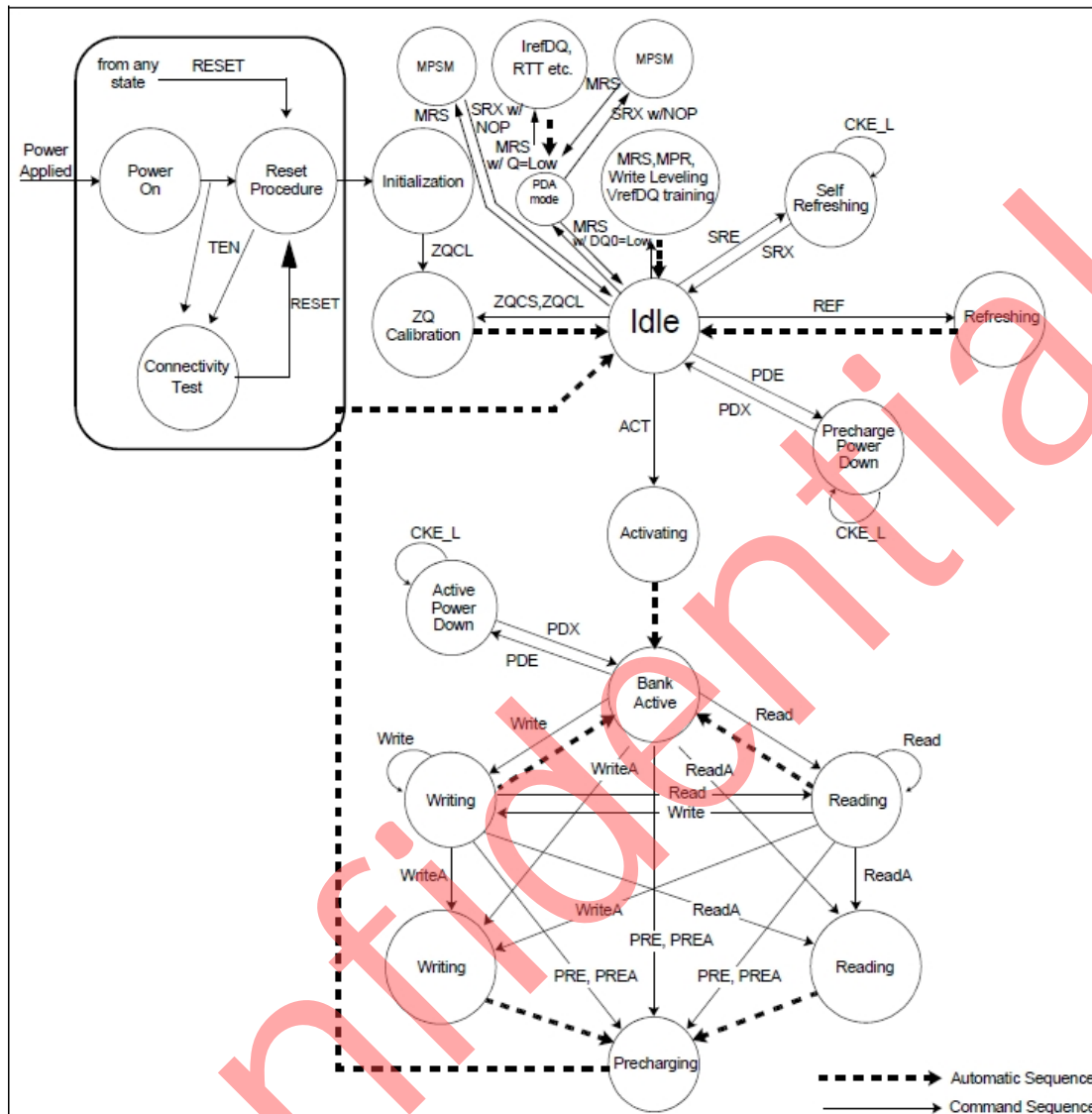
## 7 8Gb DDR4 DRAM Addressing

Table 7 - 8Gb DDR4 SDRAM Addressing

Configuration		1G x 8	512 M x 16
Bank Address	# of Bank Groups	4	2
	BG Address	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1
Row Address		A0~A15	A0~A15
Column Address		A0~A9	A0~A9
Page size		1KB	2KB

## 8 Function Description

### 8.1 Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
<b>ACT</b>	Activate	Read	RD,RDS4,RDS8	PDE	Enter Power-down
<b>PRE</b>	Precharge	Read A	RDA,RDAS4,RDAS8	PDX	Exit Power-down
<b>PREA</b>	PRECHARGE All	Write	WR,WRS4,WRS8, with/without CRC	SRE	Self-Refresh entry
<b>MRS</b>	Mode Register Set	Write A	WRA,WRAS4,WRAS8, with/without CRC	SRX	Self-Refresh exit
<b>REF</b>	Refresh,Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
<b>TEN</b>	Boundary Scan Mode Enable				

## 8.2 Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses an 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

## 8.3 RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly default values for the following MR

Settings need to be defined.

Gear down mode (MR3 A[3]) : 0 = 1/2 Rate

Per DRAM Addressability (MR3 A[4]) : 0 = Disable

Max Power Saving Mode (MR4 A[1]) : 0 = Disable

CS to Command/Address Latency (MR4 A[8:6]) : 000 = Disable

CA Parity Latency Mode (MR5 A[2:0]) : 000 = Disable

Hard Post Package Repair mode (MR4 A[13]) : 0 = Disable

Soft Post Package Repair mode (MR4 A[5]) : 0 = Disable

### 8.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization and is shown in Figure 6 in JESD79-4B .

1. Apply power (RESET\_n and TEN are recommended to be maintained below  $0.2 \times VDD$ ; all other inputs may be undefined). RESET\_n needs to be maintained below  $0.2 \times VDD$  for minimum 200us with stable power and TEN needs to be maintained below  $0.2 \times VDD$  for minimum 700us with stable power. CKE is pulled "Low" anytime before RESET\_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD min must be no greater than 200ms; and during the ramp,  $VDD \geq VDDQ$  and  $(VDD-VDDQ) < 0.3 V$ . VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

- VDD and VDDQ are driven from a single power converter output, AND

- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.76V max once power ramp is finished, AND
  - VrefCA tracks VDD/2.
- or
- Apply VDD without any slope reversal before or at the same time as VDDQ.
  - Apply VDDQ without any slope reversal before or at the same time as VTT & VrefCA.
  - Apply VPP without any slope reversal before or at the same time as VDD.
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After RESET\_n is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
  3. Clocks (CK\_t, CK\_c) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a Deselect command must be registered (with tIS set up time to clock) at clock edge Td. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
  4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as RESET\_n is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET\_n deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT\_NOM is to be enabled in MR1 the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
  5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR= Max (tXS, 5nCK)].
  6. Issue MRS Command to load MR3 with all application settings (To issue MRS command to MR3, provide "Low" to BG0, "High" to BA1, BA0)
  7. Issue MRS Command to load MR6 with all application settings (To issue MRS command to MR6, provide "Low" to BA0, "High" to BG0, BA1).
  8. Issue MRS Command to load MR5 with all application settings (To issue MRS command to MR5, provide "Low" to BA1, "High" to BG0, BA0).
  9. Issue MRS Command to load MR4 with all application settings (To issue MRS command to MR4, provide "Low" to BA1, BA0, "High" to BG0).
  10. Issue MRS Command to load MR2 with all application settings (To issue MRS command to MR2, provide "Low" to BG0, BA0, "High" to BA1).
  11. Issue MRS Command to load MR1 with all application settings (To issue MRS command to MR1, provide "Low" to BG0, BA1, "High" to BA0).
  12. Issue MRS Command to load MR0 with all application settings (To issue MRS command to MR0, provide "Low" to BG0, BA1, "High" to BA0).
  13. Issue ZQCL command to starting ZQ calibration.
  14. Wait for both tDLLK and tZQ init completed.
  15. The DDR4 SDRAM is now ready for read/write training (include Vref training and Wirte leveling).

## 8.3.2 VDD Slew rate at Power-up Initialization Sequence

Table 8 - VDD Slew Rate

Symbol	Min	Max	Units
VDD sl <sup>a</sup>	0.004	600	V/ms <sup>b</sup>
VDD_on <sup>a</sup>	TBD	200	ms <sup>c</sup>

**Note:**

- Measurement made between 300mv and 80% Vdd minimum.
- 20MHz bandlimited measurement.
- Maximum time to ramp VDD from 300mv to VDD minimum.

## 8.3.3 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization as shown in Figure 7 in JESD79-4B.

- Asserted RESRT\_n below 0.2 x VDD anytime when reset is needed (all other inputs may be undefined). RESET\_n needs to be maintained for minimum tPW\_RESET. CKE is pulled "LOW" before RESET\_n being de-asserted (min. time 10ns).
- Follow steps 2 to 10 in "Power-up Initialization Sequence" on 7.3.1.
- The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include Vref training and Write leveling).

## 8.4 Mode Register

**MR0**

Address	Operating Mode	Description	
<b>BG1</b>	RFU	0 = must be programmed to 0 during MRS	
<b>BG0, BA1:BA0</b>	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW <sup>1</sup>
<b>A17</b>	RFU	0 = must be programmed to 0 during MRS	
<b>A13<sup>5</sup>, [A11:A9]</b>	WR and RTP <sup>2,3</sup>	Write Recovery and Read to Precharge for auto precharge(see Table 9)	
<b>A8</b>	DLL Reset	0 = NO	1 = Yes
<b>A7</b>	TM	0 = Normal	1 = Test
<b>A12, A6:A4, A2</b>	CAS Latency <sup>4</sup>	(see Table 10)	
<b>A3</b>	Read Burst Type	0 = Sequential	1 = Interleave
<b>A1:A0</b>	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved	Abbreviated BL8MRS Abbreviated BC4OTF or BL8OTF Abbreviated BC4MRS

**Note:**

- Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0=111 and doesn't respond. When RFU MR Code setting is inputted, DRAM operation is not defined.
- WR (write recovery for autoprerecharge) min in clock cycles is calculated following rounding algorithm defined in Section 15.5. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR

value is used with tRP to determine tDAL.

3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
4. The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speed bin tables for each frequency. Cas Latency controlled by A12 is optional for 4Gb device.
5. A13 for WR and RTP setting is optional for 4Gb.

**Table 9 - Write Recovery and Read to Precharge (cycles)**

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

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Table 10 - CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	reserved
1	0	0	0	1	26
1	0	0	1	0	reserved
1	0	0	1	1	28
1	0	1	0	0	reserved
1	0	1	0	1	30
1	0	1	1	0	reserved
1	0	1	1	1	32
1	1	0	0	0	reserved

## MR1

Address	Operating Mode	Description
<b>BG1</b>	RFU	0 = must be programmed to 0 during MRS
<b>BG0, BA1:BA0</b>	MR Select	000 = MR0                      100 = MR4 001 = MR1                      101 = MR5 010 = MR2                      110 = MR6 011 = MR3                      111 = RCW <sup>3</sup>
<b>A17</b>	RFU	0 = must be programmed to 0 during MRS
<b>A13</b>	RFU	0 = must be programmed to 0 during MRS
<b>A12</b>	Qoff <sup>1</sup>	0 = Output buffer enabled 1 = Output buffer disabled
<b>A11</b>	TDQS enable	0 = Disable                      1 = Enable
<b>A10, A9, A8</b>	RTT_NOM	(see Table 11)
<b>A7</b>	Write Leveling Enable	0 = Disable                      1 = Enable
<b>A6, A5</b>	RFU	0 = must be programmed to 0 during MRS
<b>A4, A3</b>	Additive Latency	00 = 0(AL disabled)            10 = CL-2 01 = CL-1                      11 = Reserved
<b>A2, A1</b>	Output Driver Impedance Control	(see Table 12)
<b>A0</b>	DLL Enable	0 = Disable <sup>2</sup> 1 = Enable

### Note:

1. Outputs disabled – DQS, DQS\_ts, DQS\_cs.
2. States reversed to “0 as Disable” with respect to DDR4.
3. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

**Table 11 - RTT\_NOM**

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

**Table 12 - Output Driver Impedance Control**

A2	A1	RTT_NOM
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

## MR2

Address	Operating Mode	Description
<b>BG1</b>	RFU	0 = must be programmed to 0 during MRS
<b>BG0, BA1:BA0</b>	MR Select	000 = MR0                      100 = MR4 001 = MR1                      101 = MR5 010 = MR2                      110 = MR6 011 = MR3                      111 = RCW <sup>1</sup>
<b>A17</b>	RFU	0 = must be programmed to 0 during MRS
<b>A13</b>	RFU	0 = must be programmed to 0 during MRS
<b>A12</b>	Write CRC	0 = Disable                      1 = Enable <sup>23</sup>
<b>A11, A10:A9</b>	RTT_WR	(see Table 13)
<b>A8, A2</b>	RFU	0 = must be programmed to 0 during MRS
<b>A7:A6</b>	Low Power Auto Self Refresh(LPASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode(Auto Self Refresh)
<b>A5:A3</b>	CAS Write Larency(CWL)	(see Table 14)
<b>A1:A0</b>	RFU	0 = must be programmed to 0 during MRS

### Note:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. After the WCRC error, the user can use the MPR to read the CRC err status information, but the next WCRC error want to be recorded in the MPR, a write without the WCRC error must be initiated, otherwise even if the MRS configuration CRC Error Clear is inserted, it does not work.
3. For a x16, when the DRAM detects an error in CRC tree, DDR4 DRAMs will mask all DQs.

**Table 13 - RTT\_WR**

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

**Table 14 - CWL (CAS Write Latency)**

A5	A4	A3	CWL	Operating Data Rate in MT/s for 1 tCK Write Preamble		Operating Data Rate in MT/s for 2 tCK Write Preamble <sup>1</sup>	
				1 <sup>st</sup> set	2 <sup>nd</sup> set	1 <sup>st</sup> set	2 <sup>nd</sup> set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	2933 / 3200	2400	2666	2400
1	1	0	18		2666	2933 / 3200	2666
1	1	1	20		2933 / 3200		2933 / 3200

**Note:**

1. The 2 tCK Write Preamble is valid for DDR4-2400/2666/2933/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

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## MR3

Address	Operating Mode	Description
<b>BG1</b>	RFU	0 = must be programmed to 0 during MRS
<b>BG0, BA1:BA0</b>	MR Select	000 = MR0                      100 = MR4 001 = MR1                      101 = MR5 010 = MR2                      110 = MR6 011 = MR3                      111 = RCW <sup>1</sup>
<b>A17</b>	RFU	0 = must be programmed to 0 during MRS
<b>A13</b>	RFU	0 = must be programmed to 0 during MRS
<b>A12:A11</b>	MPR Read Format	0 = Serial                      10 = Staggered 01 = Parallel                      11 = Reserved
<b>A10:A9</b>	Write CMD Latency when CRC and DM are enabled	(see Table 16)
<b>A8:A6</b>	Fine Granularity Refresh Mode	(see Table 15)
<b>A5</b>	Temperature sensor readout	0 = Disable                      1 = Enable
<b>A4</b>	Per DRAM Addressability	0 = Disable                      1 = Enable <sup>2</sup>
<b>A3</b>	Geardown Mode	0 = 1/2 Rate                      1 = 1/4 Rate
<b>A2</b>	MPR Operation	0 = Normal                      1 = Dataflow from/to MPR
<b>A1:A0</b>	MPR page Selection	00 = Page0                      10 = Page2 01 = Page1                      11 = Page3 (see Table 17)

### Note:

- Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
- If entering PDA mode with MRS configed to the BurstLength in OTF(MR0[1:0]=0b01) mode, SOC should config MR0[1:0]=0b01 to the BurstLenth in OTF mode again after exiting PDA;

**Table 15 - Fine Granularity Refresh Mode**

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal(Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

**Table 16 - MR3 A<10:9> Write Command Latency when CRC and DM are both enabled**

A10	A9	CRC+DM Write Command Latency	Operating Data Rate
0	0	4nCK	1600
0	1	5nCK	1866,2133,2400,2666
1	0	6nCK	2933,3200
1	1	RFU	RFU

**Table 17 - MPR Data Format**

MPR page0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page1 (CA Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-only
	01 = MPR1	CAS_n/A15	WE_n/A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS_n/A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency <sup>4</sup>			C[2]	C[1]	C[0]	
				MR5. A[2]	MR5. A[1]	MR5. A[0]				

**Note:**

1. MPR used for C/A parity error log readout is enabled by setting A[2] in MR3.
2. For 8Gb DDR4, where A[17] is not used, MPR2[1] should be treated as don't care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.
4. MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note	
BA1:BA0	00 = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status		CRC Write Enable	Rtt_WR		Read-only	
		-	-	MR2	-	-	MR2	MR2			
				A11	-	-	A12	A10	A9		
	01 = MPR1	Vref DQ Tmg range	Vref DQ training Value						Geardown Enable		
		MR6	MR6						MR3		
		A6	A5	A4	A3	A2	A1	A0	A3		
	10 = MPR2	CAS Latency				CAS Write Latency					
		MR0				MR2					
		A6	A5	A4	A2	A12	A5	A4	A3		
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance			
		MR1			MR5			MR1			
		A10	A9	A6	A8	A7	A6	A2	A1		

**Note:**

- MR bit for Temperature Sensor Readout.
- MR3 bit A5 = 1: DRAM updates the temperature sensor status to MPR Page2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.
- MR3 bit A5 = 0: DRAM disables updates to the temperature sensor status in MPR Page2 (MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh(> tREFI)
0	1	1X refresh rate(= tREFI)
1	0	2X refresh rate(1/2*tREFI)
1	1	rsvd

MPR page3 (Vendor use only)1

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	Read-only
	01 = MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	11 = MPR3	don't care	don't care	don't care	don't care	MAC	MAC	MAC	MAC	

## MR4

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0                      100 = MR4 001 = MR1                      101 = MR5 010 = MR2                      110 = MR6 011 = MR3                      111 = RCW <sup>1</sup>
A17	RFU	0 = must be programmed to 0 during MRS
A13	hPPR	0 = Disable                      1 = Enable
A12	Write Preamble	0 = 1 nCK                      1 = 2 nCK
A11	Read Preamble	0 = 1 nCK                      1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable                      1 = Enable
A9	Self Refresh Abort	0 = Disable                      1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode(cycles)	000 = Disable                      100 = 6 001 = 3                              101 = 8 010 = 4                              110 = Reserved 011 = 5                              111 = Reserved (see Table 18)
A5	sPPR	0 = Disable                      1 = Enable
A4	Internal Vref Monitor	0 = Disable                      1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable                      1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal                      1 = Extended
A1	Maximum Power Down Mode <sup>1</sup>	0 = Disable                      1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

**Note:** Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn't respond. When PFU MR Code setting is inputted, DRAM operation is not defined.

- When exit Maximum-Power-Down-Mode, DLL must be reset or a complete initialization process needs to be completed in system.

**Table 18 - CS to CMD / ADDR Latency Mode Setting**

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

## MR5

Address	Operating Mode	Description
<b>BG1</b>	RFU	0 = must be programmed to 0 during MRS
<b>BG0, BA1:BA0</b>	MR Select	000 = MR0                      100 = MR4 001 = MR1                      101 = MR5 010 = MR2                      110 = MR6 011 = MR3                      111 = RCW <sup>1</sup>
<b>A17</b>	RFU	0 = must be programmed to 0 during MRS
<b>A13</b>	RFU	0 = must be programmed to 0 during MRS
<b>A12</b>	Read DBI	0 = Disable                      1 = Enable
<b>A11</b>	Write DBI	0 = Disable                      1 = Enable
<b>A10</b>	Data Mask	0 = Disable                      1 = Enable
<b>A9</b>	CA parity Persistent Error	0 = Disable                      1 = Enable
<b>A8:A6</b>	RTT_PARK	(see Table 19)
<b>A5</b>	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
<b>A4</b>	C/A Parity Error Status	0 = Clear                      1 = Error
<b>A3</b>	CRC Error Clear	0 = Clear                      1 = Error
<b>A2:A0</b>	C/A Parity Latency Mode	(see Table 20)

### Note:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn't respond. When PFU MR Code setting is inputted, DRAM operation is not defined.
2. When RTT\_NOM Disable is set in MR1, A5 of MR5 will be ignored.

**Table 19 - RTT\_PARK**

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

**Table 20 - C/A Parity Latency Mode**

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	
0	0	1	4	1600,1866,2133
0	1	0	5	2400,2666
0	1	1	6	2933,3200
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

**Note:** Parity Latency must be programmed according to timing parameters by speed grade table.

### MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0                      100 = MR4 001 = MR1                      101 = MR5 010 = MR2                      110 = MR6 011 = MR3                      111 = RCW <sup>1</sup>
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A10	tCCD_L	(see Table 17)
A9,A8	RFU	0 = must be programmed to 0 during MRS
A7	VrefDQ Training Enable	0 = Disable (Normal operation Mode) 1 = Enable (Training Mode)
A6	VrefDQ Training Range	(see Table 22)
A5:A0	VrefDQ Training Value	(see Table 23)

**Note:** Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1; BA0 = 111 and doesn't respond.

**Table 21 - tCCD\_L and tDLLK**

A12	A11	A10	tCCD_L.min(nCK) <sup>1</sup>	tDLL_K.min(nCK) <sup>1</sup>	Note
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps < Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	2400Mbps < Data rate ≤ 2666Mbps (2666Mbps)
1	0	0	8		2666Mbps < Data rate ≤ 3200Mbps (2933/3200Mbps)
1	0	1	Reserved		
1	1	0			
1	1	1			

**Note:** tCCD\_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency.

**Table 22 - VrefDQ Training: Range**

A6	VrefDQ Range
0	Range 1
1	Range 2

**Table 23 - VrefDQ Training: Values**

A5:A0	Range1	Range2	A5:A0	Range1	Range2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	66.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111	Reserved	Reserved

**MR7 DRAM: Ignore**

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM. Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

## 8.5 Per DRAM Addressability

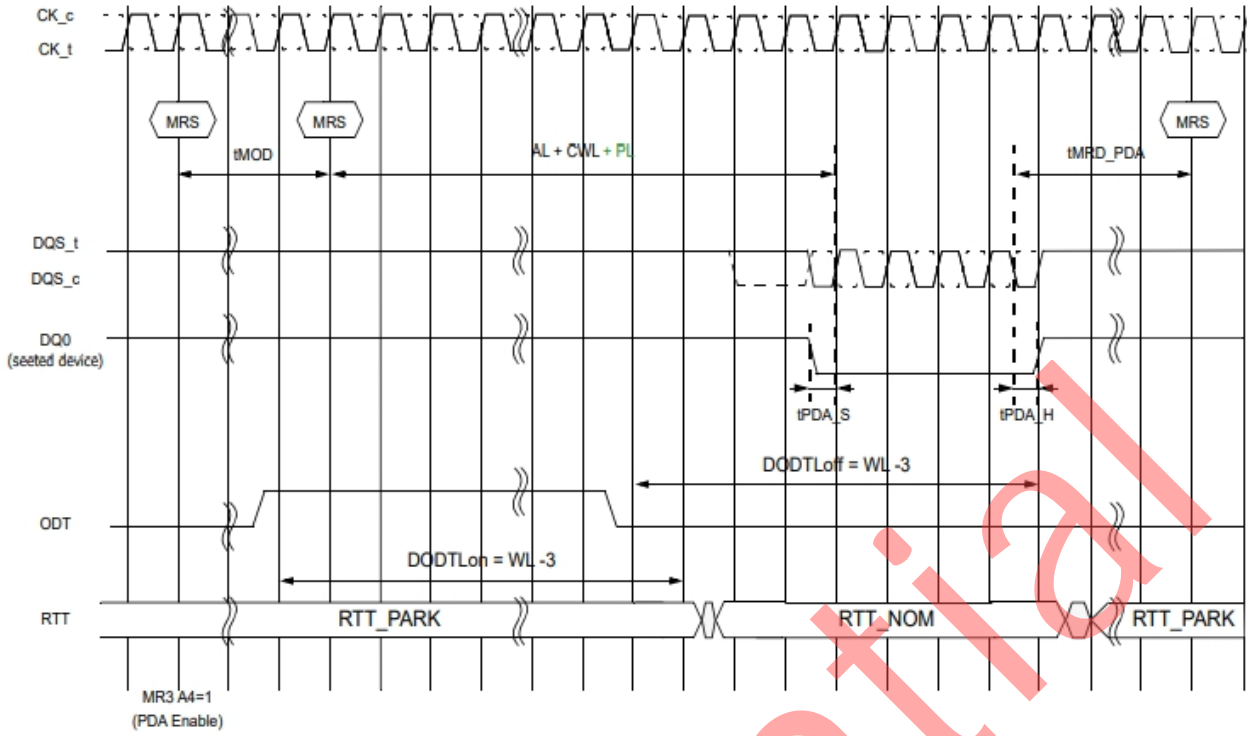
DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank.

1. Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required.
2. Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible. - RTT\_PARK MR5 {A8:A6} = Enable - RTT\_NOM MR1 {A10:A9:A8} = Enable
3. Enable 'per DRAM addressability (PDA)' mode using MR3 bit "A4=1".
4. In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0 for x4 and x8, and DQL0 for x16. DRAM captures DQ0 for x4 and x8, and DQL0 for x16 by using DQS\_c and DQS\_t for x4 and x8, DQSL\_c and DQSL\_t for x16 signals as shown Figure 35.. If the value on DQ0 for x4 and x8, and DQL0 for x16 is 0 then the DRAM executes the MRS command. If the value on DQ0 is 1, then the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired devices and mode registers using MRS command and DQ0 for x4 and x8, and DQL0 for x16.
6. In the 'per DRAM addressability' mode, only MRS commands are allowed.
7. The mode register set command cycle time at PDA mode,  $AL + CWL + BL/2 - 0.5tCK + tMRD\_PDA + (PL)$  is required to complete the write operation to the mode register and is the minimum time required between two MRS commands in Figure 35..
8. Remove the DRAM from 'per DRAM addressability' mode by setting MR3 bit "A4=0". (This command will require DQ0=0 for x4 and x8, and DQL0 for x16 in Figure 36..

NOTE Removing a DRAM from per DRAM addressability mode will require programming the entire MR3 when the MRS command is issued. This may impact some per DRAM values programmed within a rank as the exit command is sent to the rank. In order to avoid such a case the PDA Enable/Disable Control bit is located in a mode register that does not have any 'per DRAM addressability' mode controls). In per DRAM addressability mode, DRAM captures DQ0 for x4 and x8, and DQL0 for x16 using DQS\_t and DQS\_c for x4 and x8, DQSL\_c and DQSL\_t for x16 like normal write operation. However, Dynamic ODT is not supported. So extra care required for the ODT setting. If RTT\_NOM MR1 {A10:A9:A8} = Enable, DDR4 SDRAM data termination need to be controlled by ODT pin and apply the same timing parameters as defined in Direct ODT function that shown in Table 80. VrefDQ value must be set to either its midpoint or Vcent\_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

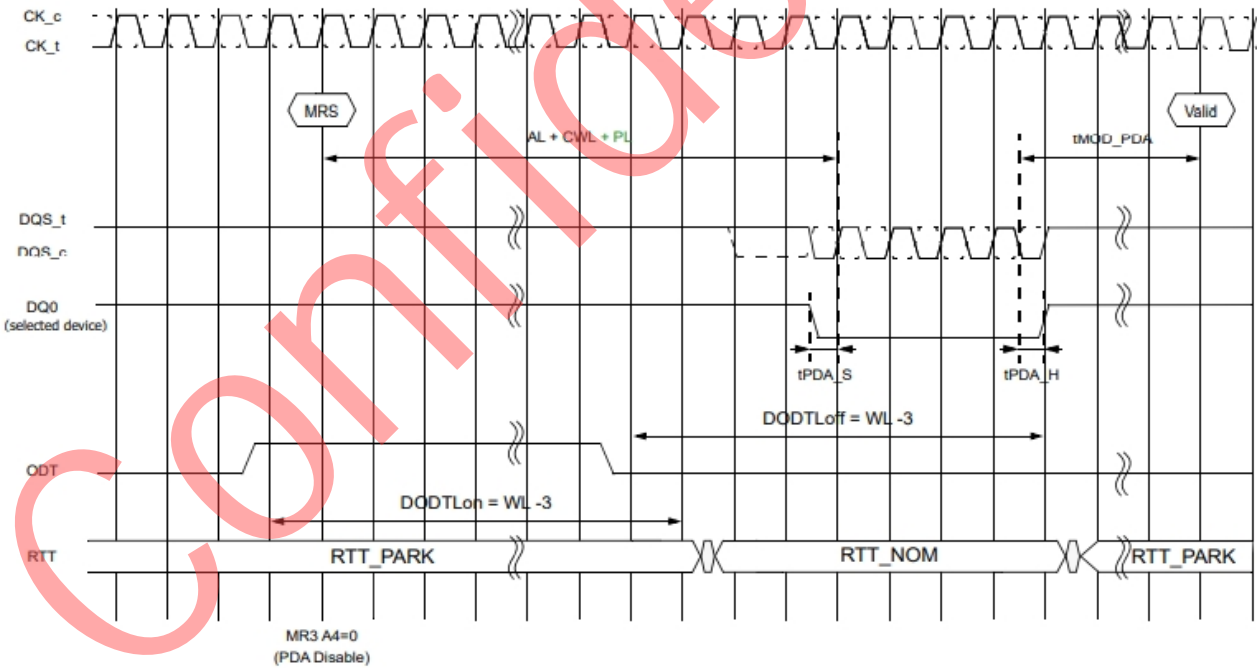
**Table 80 — Applied ODT Timing Parameter to PDA Mode**

Symbol	Parameter
<b>DODTLon</b>	Direct ODT turn on latency
<b>DODTLoFF</b>	Direct ODT turn off latency
<b>tADC</b>	RTT change timing skew
<b>tAONAS</b>	Asynchronous RTT_NOM turn-on delay
<b>tAOFAS</b>	Asynchronous RTT_NOM turn-off delay



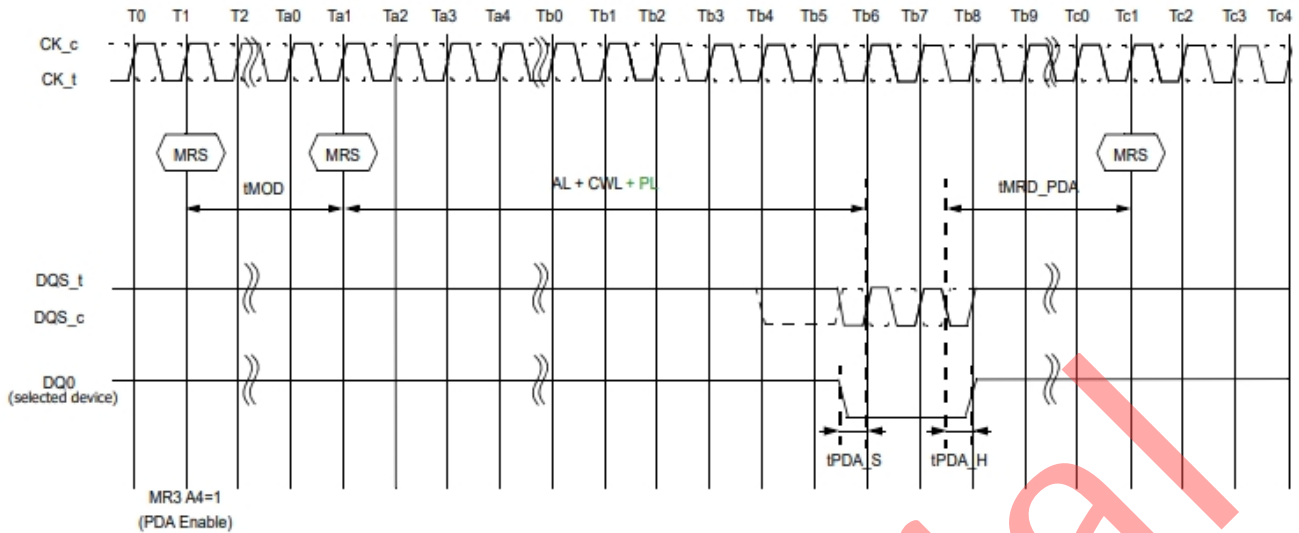
NOTE RTT\_PARK = Enable, RTT\_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON, CA parity is used

Figure 35 — MRS w/ per DRAM addressability (PDA) issuing before MRS



NOTE RTT\_PARK = Enable, RTT\_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON, CA parity is used

Figure 36 — MRS w/ per DRAM addressability (PDA) Exit



**NOTE** CA parity is used.

**Figure 37 — PDA using Burst Chop 4**

Since PDA mode may be used to program optimal Vref for the DRAM, the DRAM may incorrectly read DQ level at the first DQS edge and the last falling DQS edge. It is recommended that DRAM samples DQ0 or DQL0 on either the first falling or second rising DQS edges. This will enable a common implementation between BC4 and BL8 modes on the DRAM. Controller is required to drive DQ0 or DQL0 to a 'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

## 8.6 Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the tDQSS, tDSS and tDSH specifications.

The memory controller can use the 'write leveling' feature and feedback from the DDR4 SDRAM to adjust the DQS\_t - DQS\_c to CK\_t - CK\_c relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS\_t - DQS\_c to align the rising edge of DQS\_t - DQS\_c with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK\_t - CK\_c, sampled with the rising edge of DQS\_t - DQS\_c, through the DQ bus. The controller repeatedly delays DQS\_t - DQS\_c until a transition from 0 to 1 is detected. The DQS\_t - DQS\_c delay established through this exercise would ensure tDQSS specification.

Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS\_t - DQS\_c signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme in Figure 14.

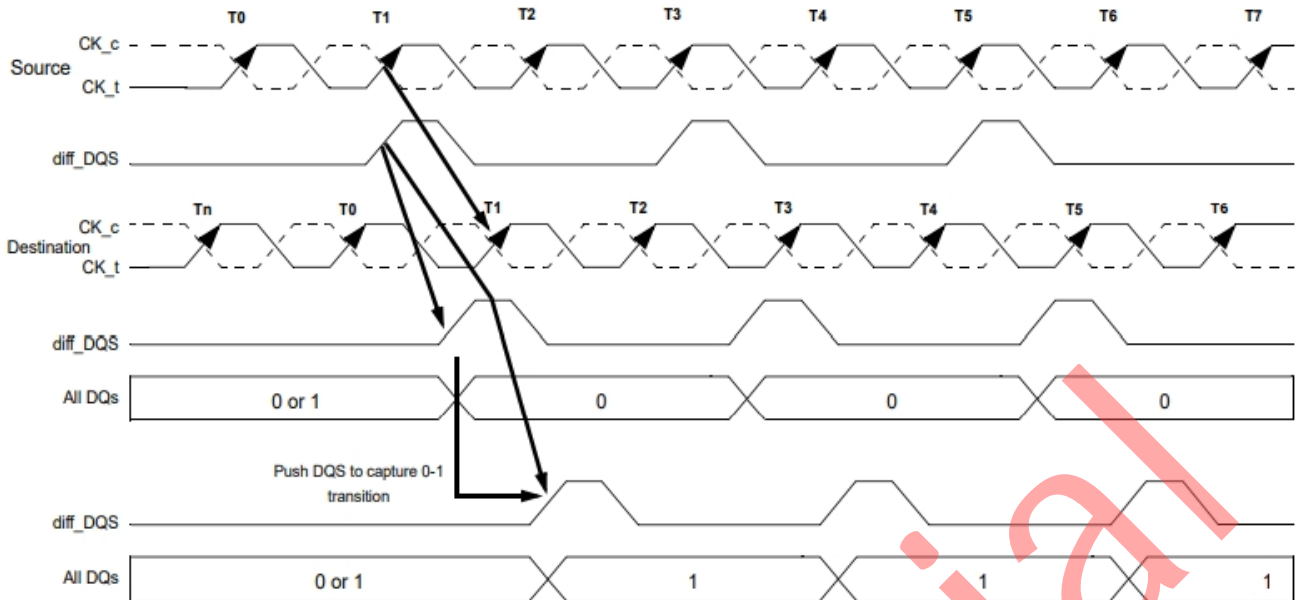


Figure 14 — Write Leveling Concept

DQS\_t - DQS\_c driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller. All data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff\_DQS(diff\_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff\_DQS(diff\_LDQS) to clock relationship.

## 8.7 CRC

(TBD)

## 9 Absolute Maximum Ratings

### 9.1 Absolute Maximum DC Ratings

Table 24 - DDR4 SDRAM Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
VIN, VOUT	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3
TSTG	Storage Temperature	-55 to +100	°C	1,2

**Note:**

- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV.
- VPP must be equal or greater than VDD/VDDQ at all times.

## 9.2 DRAM Component Operating Temperature Range

Table 25 - DDR4 SDRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3

**Note:**

- Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 – 85 °C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the refresh interval t<sub>REFI</sub> to 3.9us.
  - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b).

## 10 DC Operating Conditions

Table 26 - Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

**Note:**

- Under all conditions V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.
- V<sub>DDQ</sub> tracks with V<sub>DD</sub>. AC parameters are measured with V<sub>DD</sub> and V<sub>DDQ</sub> tied together.
- DC bandwidth is limited to 20MHz

## 11 AC & DC Input Measurement Levels

### 11.1 AC & DC Logic Input Levels for Single-ended Signals

Table 27 - Single-ended AC & DC input Levels for Command and Address

Symbol	Parameter	DDR4-2400		DDR4-2666/2933/3200		Unit
		Min.	Max.	Min.	Max.	
$V_{IH.CA(DC75)}$	DC input logic high	VREFCA+75	VDD	VREF+65	VDD	mV
$V_{IL.CA(DC75)}$	DC input logic low	VSS	VREFCA-75	VSS	VREF-65	mV
$V_{IH.CA(AC100)}$	AC input logic high <sup>1</sup>	VREF+100	Note2	VREF+90	VDD	mV
$V_{IL.CA(AC100)}$	AC input logic low <sup>1</sup>	Note2	VREF-100	VSS	VREF-90	mV
$V_{REFCA(DC)}$	Reference Voltage for ADD, CMD inputs <sup>2,3</sup>	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V

**Note:**

1. See "Overshoot and Undershoot Specifications" in 10.3
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than  $\pm 1\%$  VDD (for reference: approx.  $\pm 12\text{mV}$ )
3. for reference: approx.  $VDD/2 \pm 12\text{mV}$

## 11.2 AC & DC Input Measurement Levels: VREF Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages VREFCA is illustrated in Figure 1. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 27. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than  $\pm 1\% V_{DD}$ .

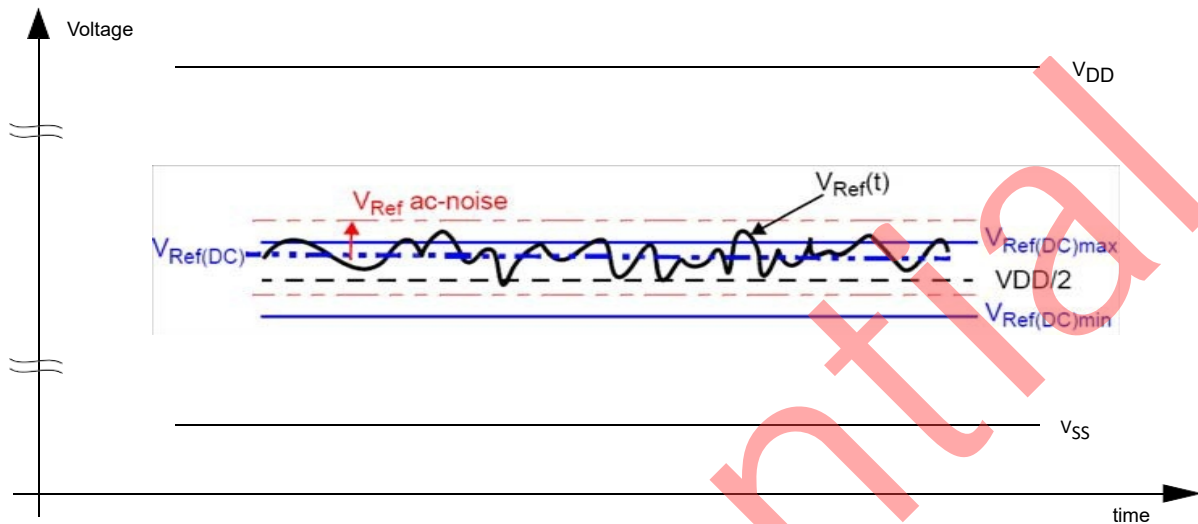


Figure 1 - Illustration of VREF(DC) tolerance and VREF AC-noise limits

The voltage levels for setup and hold time measurements  $V_{IH}(AC)$ ,  $V_{IH}(DC)$ ,  $V_{IL}(AC)$  and  $V_{IL}(DC)$  are dependent on  $V_{REF}$ . " $V_{REF}$ " shall be understood as  $V_{REF}(DC)$ , as defined in Figure 1.

This clarifies, that DC-variations of  $V_{REF}$  affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for  $V_{REF}(DC)$  deviations from the optimum position within the data-eye of the input signals

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with  $V_{REF}$  AC-noise. Timing and voltage effects due to AC-noise on  $V_{REF}$  up to the specified limit ( $\pm 1\%$  of  $V_{DD}$ ) are included in DRAM timings and their associated deratings.

## 11.3 AC and DC Logic Input Levels for Differential Signals

### 11.3.1 Differential signal definition

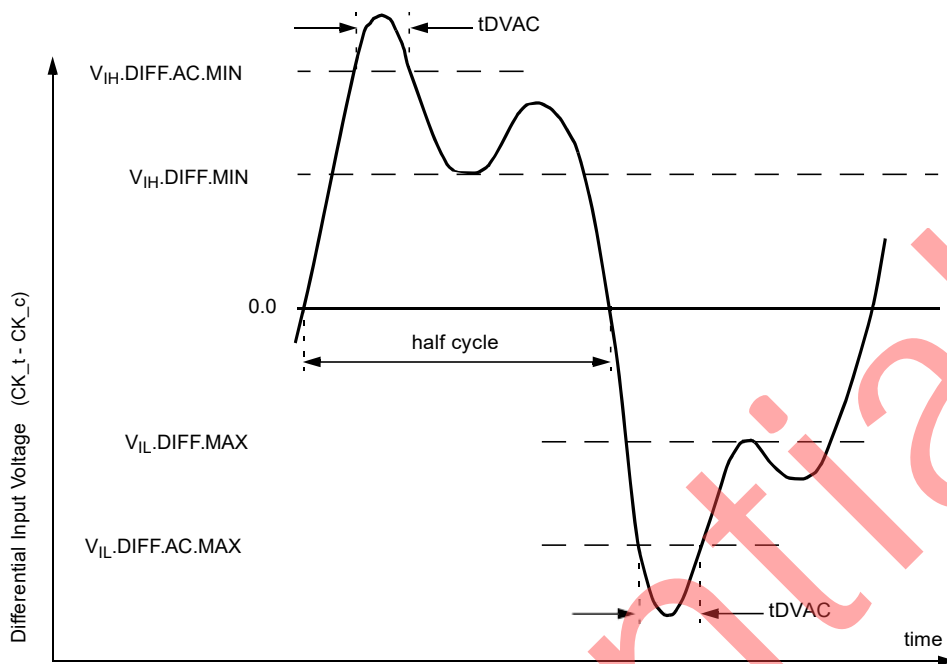


Figure 2 - Definition of differential ac-swing and “time above ac-level” tDVAC

**Note:**

1. Differential signal rising edge from  $V_{IL,DIFF,MAX}$  to  $V_{IH,DIFF,MIN}$  must be monotonic slope.
2. Differential signal falling edge from  $V_{IH,DIFF,MIN}$  to  $V_{IL,DIFF,MAX}$  must be monotonic slope.

### 11.3.2 Differential Swing Requirements for Clock (CK\_t - CK\_c)

Table 28 - Differential AC & DC Input Levels

Symbol	Parameter	DDR4-2400,2666,2933,3200		Unit	NOTE
		Min	Max		
$V_{IH,diff}$	differential input high	0.120	NOTE 3	V	1
$V_{IL,diff}$	differential input low	NOTE 3	-0.120	V	1
$V_{IH,diff}(AC)$	differential input high ac	$2 \times (V_{IH}(AC) - V_{REF})$	NOTE 3	V	2
$V_{IL,diff}(AC)$	differential input low ac	NOTE 3	$2 \times (V_{IL}(AC) - V_{REF})$	V	2

**Note:**

1. Used to define a differential signal slew-rate.
2. for CK\_t - CK\_c use  $V_{IH,CA}/V_{IL,CA}(AC)$  of ADD/CMD and  $V_{REF,CA}$
3. These values are not defined; however, the differential signals CK\_t - CK\_c, need to be within the respective limits ( $V_{IH,CA}(DC)$  max,  $V_{IL,CA}(DC)$  min) for single-ended signals as well as the limitations for overshoot and undershoot

**Table 29 - Allowed Time Before Ringback (tDVAC) for CK\_t - CK\_c**

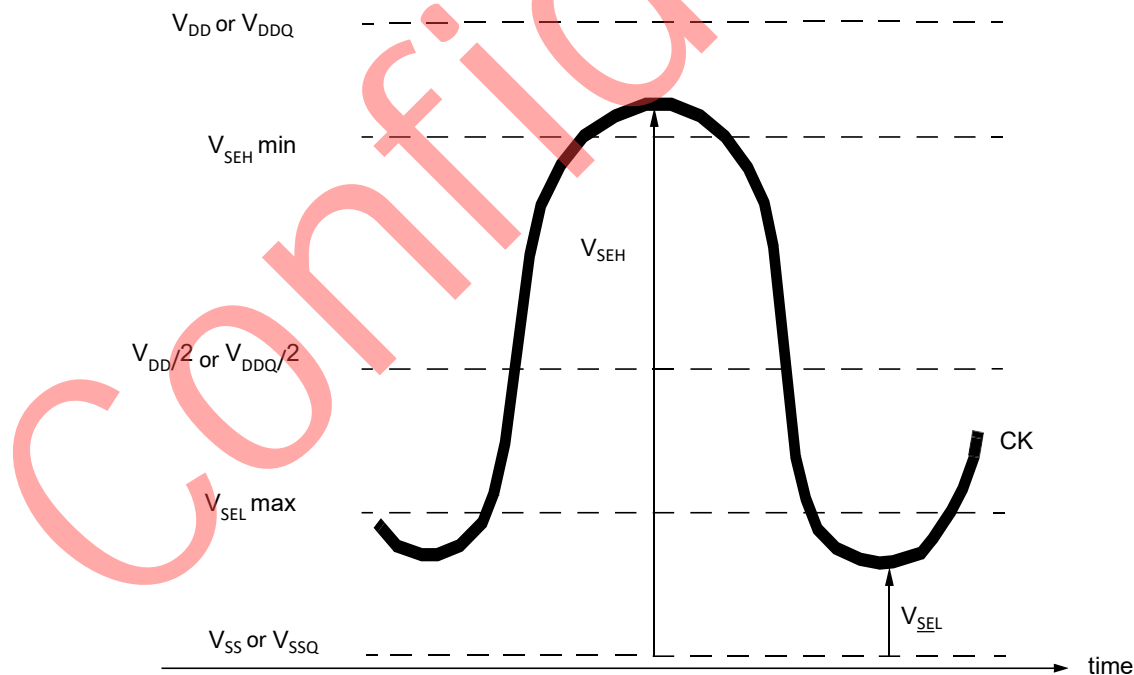
Slew Rate [V/ns]	tDVAC [ps] @  VIH/Ldiff(AC)  = 200mV		tDVAC [ps] @  VIH/Ldiff(AC)  = TBDmV	
	Min	Max	Min	Max
> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
< 1.0	80	-	TBD	-

### 11.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK\_t, CK\_c) has also to comply with certain requirements for single-ended signals.

CK\_t and CK\_c have to approximately reach  $V_{SEHmin} / V_{SELmax}$  (approximately equal to the ac-levels  $\{V_{IH,CA}(AC) / V_{IL,CA}(AC)\}$  for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g. if Different value than  $V_{IH,CA}(AC100)/V_{IL,CA}(AC100)$  is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK\_t and CK\_c .



**Figure 3 - Single-ended requirement for differential signals**

Note that, while ADD/CMD signal requirements are with respect to  $V_{refCA}$ , the single-ended components of differential signals have a requirement with respect to  $V_{DD} / 2$ ; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach  $V_{SELmax}$ ,  $V_{SEHmin}$  has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

**Table 30 - Single-ended levels for CK\_t, CK\_c**

Symbol	Parameter	DDR4-2400/2666/2933/3200		Unit	NOTE
		Min	Max		
<b>VSEH</b>	Single-ended high-level for CK_t,CK_c	(VDD/2)+90	NOTE3	mV	1,2
<b>VSEL</b>	Single-ended low-level for CK_t,CK_c	NOTE3	(VDD/2)-90	mV	1,2

**Note:**

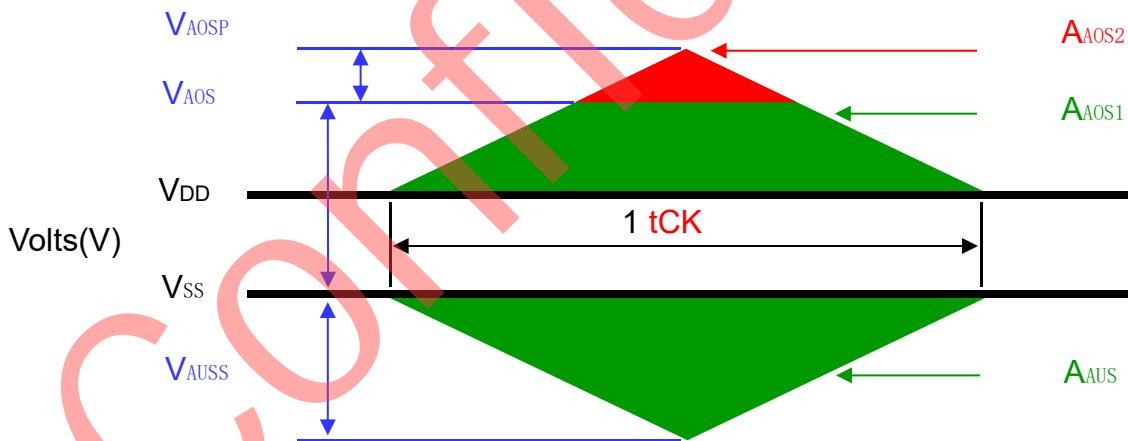
1. For CK\_t - CK\_c use  $V_{IH,CA}/V_{IL,CA}(AC)$  of ADD/CMD
2.  $V_{IH}(AC)/V_{IL}(AC)$  for ADD/CMD is based on  $V_{REFCA}$
3. These values are not defined, however the single-ended signals CK\_t - CK\_c need to be within the respective limits ( $V_{IH,CA}(DC)$  max,  $V_{IL,CA}(DC)$  min) for single-ended signals as well as the limitations for overshoot and undershoot.

### 11.3.4 Address, Command and Control Overshoot and Undershoot Specifications

**Table 31 - AC Overshoot/Undershoot Specification for Address, Command and Control Pins**

Parameter	Symbol	Specification	Unit
		2400,2666,2933,3200	
Maximum peak amplitude above $V_{AOS}$	$V_{AOSP}$	0.06	V
Upper boundary of overshoot area $A_{AOS1}$	$V_{AOS}$	VDD+0.24	V
Maximum peak amplitude allowed for undershoot	$V_{AUS}$	0.30	V
Maximum overshoot area per 1 tCK above $V_{AOS}$	$A_{AOS2}$	0.0055	V/ns
Maximum overshoot area per 1 tCK between VDD and $V_{AOS}$	$A_{AOS1}$	0.1699	V/ns
Maximum undershoot area per 1 tCK below $V_{SS}$	$A_{AUS}$	0.1762	V/ns

(A0-A13, BG0-BG1,BA0-BA1,ACT\_n,RAS\_n/A16,CAS\_n/A15,WE\_n/A14,CS\_n,CKE,ODT)



**Figure 4 - Address, Command and Control Overshoot and Undershoot Definition**

## 11.3.5 Clock Overshoot and Undershoot Specifications

Table 32 - AC Overshoot/Undershoot Specification for Clock

Parameter	Symbol	Specification	Unit
		2400,2666,2933,3200	
Maximum peak amplitude above $V_{COS}$	$V_{COSP}$	0.06	V
Upper boundary of overshoot area $A_{DOS1}$	$V_{COS}$	$V_{DD}+0.24$	V
Maximum peak amplitude allowed for undershoot	$V_{CUS}$	0.30	V
Maximum overshoot area per 1 UI above $V_{COS}$	$A_{COS2}$	0.0025	V/ns
Maximum overshoot area per 1 UI between $V_{DD}$ and $V_{DOS}$	$A_{COS1}$	0.0750	V/ns
Maximum undershoot area per 1 UI below $V_{SS}$	$A_{CUS}$	0.0762	V/ns

(CK\_t, CK\_c)

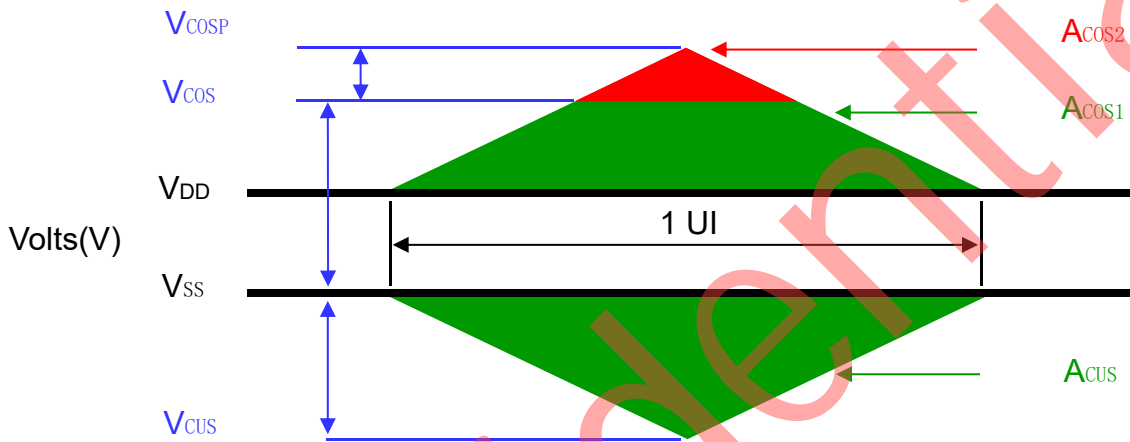


Figure 5 - Clock Overshoot and Undershoot Definition

## 11.3.6 Data, Strobe and Mask Overshoot and Undershoot Specifications

Table 33 - AC Overshoot/Undershoot Specification for Data, Strobe and Mask

Parameter	Symbol	Specification				Unit
		2400	2666	2933	3200	
Maximum peak amplitude above $V_{DOS}$	$V_{DOSP}$	0.16				V
Upper boundary of overshoot area $A_{DOS1}$	$V_{DOS}$	$V_{DDQ}+0.24$				V
Lower boundary of undershoot area $A_{DUS1}$	$V_{DUS}$	0.30				V
Maximum peak amplitude below $V_{DUS}$	$V_{DUSP}$	0.10				V
Maximum overshoot area per 1 UI above $V_{DOS}$	$A_{DOS2}$	0.0100	0.0129	0.0113	0.0100	V/ns
Maximum overshoot area per 1 UI between $V_{DDQ}$ and $V_{DOS}$	$A_{DOS1}$	0.0700	0.0900	0.0788	0.0700	V/ns
Maximum undershoot area per 1 UI between $V_{SSQ}$ and $V_{DUS1}$	$A_{DUS1}$	0.0700	0.0900	0.0788	0.0700	V/ns
Maximum undershoot area per 1 UI below $V_{DUS}$	$A_{DUS2}$	0.0100	0.0129	0.0113	0.0100	V/ns

(DQ,DQS\_t,DQS\_c,DM\_n,DBI\_n,TDQS\_t,TDQS\_c)

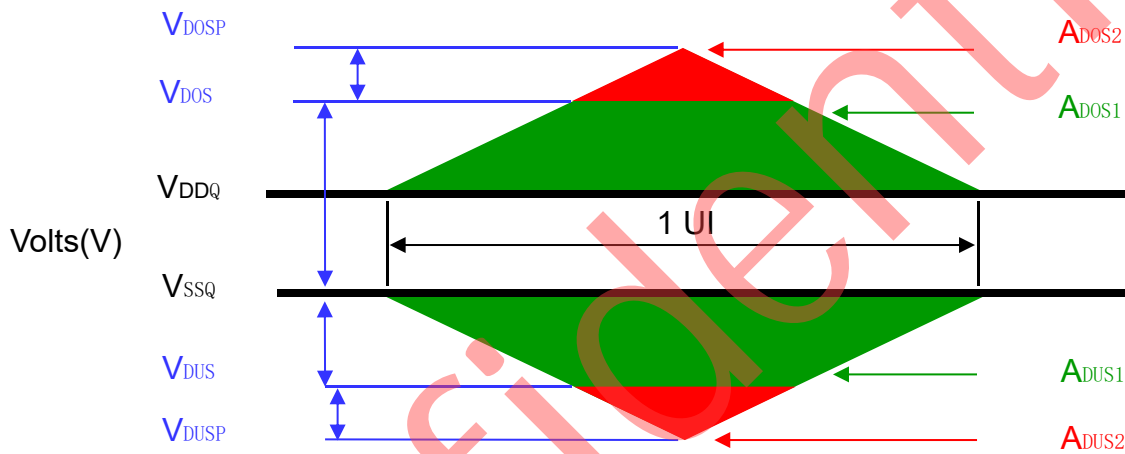


Figure 6 - Data, Strobe and Mask Overshoot and Undershoot Definition

## 11.4 Slow Rate Definitions

### 11.4.1 Slow Rate Definitions for Differential Input Signals (CK)

Input slow rate for differential signals (CK\_t, CK\_c) are defined and measured as shown in Table 34 and Figure 7.

Table 34 - Differential Input Slow Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slow rate for rising edge(CK_t - CK_c)	V <sub>ILdiffmax</sub>	V <sub>IHdiffmin</sub>	$[ V_{IHdiffmin} - V_{ILdiffmax} ] / \Delta TR_{diff}$
Differential input slow rate for falling edge(CK_t - CK_c)	V <sub>IHdiffmin</sub>	V <sub>ILdiffmax</sub>	$[ V_{IHdiffmin} - V_{ILdiffmax} ] / \Delta TF_{diff}$

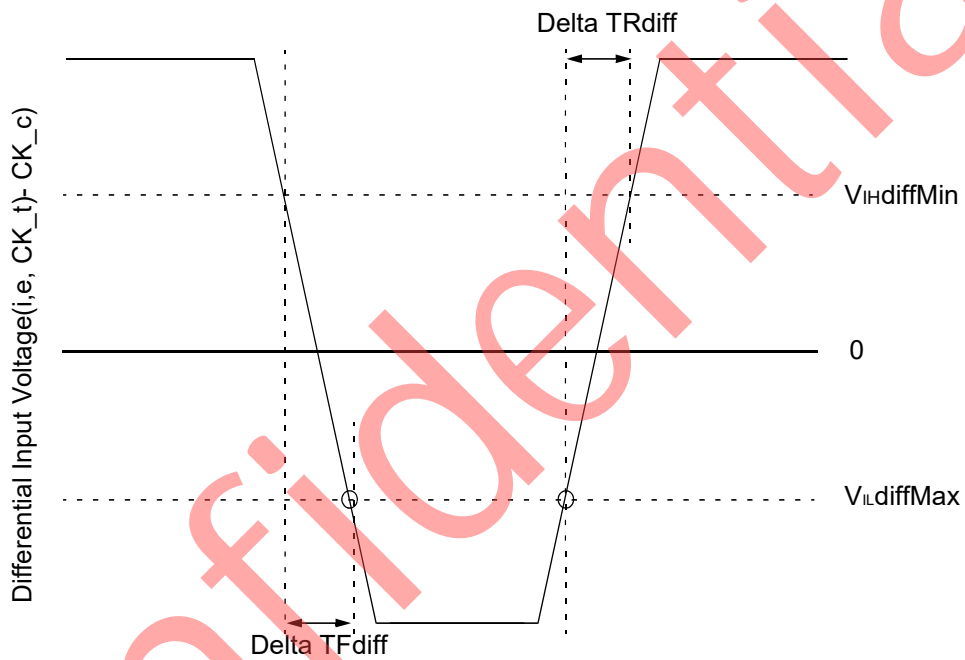
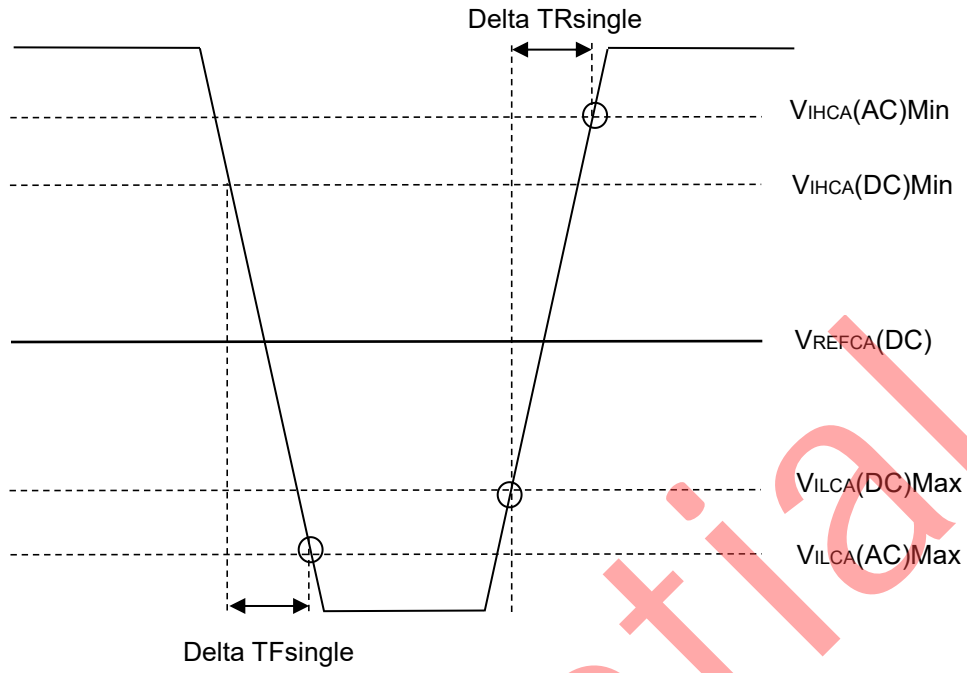


Figure 7 - Differential Input Slow Rate Definition for CK\_t, CK\_c

## 11.4.2 Slew Rate Definition for Single-ended Input Signals (CMD/ADD)



**Figure 8 - Single-ended Input Slew Rate definition for CMD and ADD**

**Note:**

1. Single-ended input slew rate for rising edge =  $\{ V_{IHCA(AC)Min} - V_{ILCA(DC)Max} \} / \Delta T_{Rsingle}$ .
2. Single-ended input slew rate for falling edge =  $\{ V_{IHCA(DC)Min} - V_{ILCA(AC)Max} \} / \Delta T_{Fsingle}$ .
3. Single-ended signal rising edge from  $V_{ILCA(DC)Max}$  to  $V_{IHCA(DC)Min}$  must be monotonic slope.
4. Single-ended signal falling edge from  $V_{IHCA(DC)Min}$  to  $V_{ILCA(DC)Max}$  must be monotonic slope.

## 11.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK\_t, CK\_c) must meet the requirements in Table 35. The differential input cross point voltage  $V_{ix}$  is measured from the actual cross point of true and complement signals to the midlevel between of  $V_{DD}$  and  $V_{SS}$ .

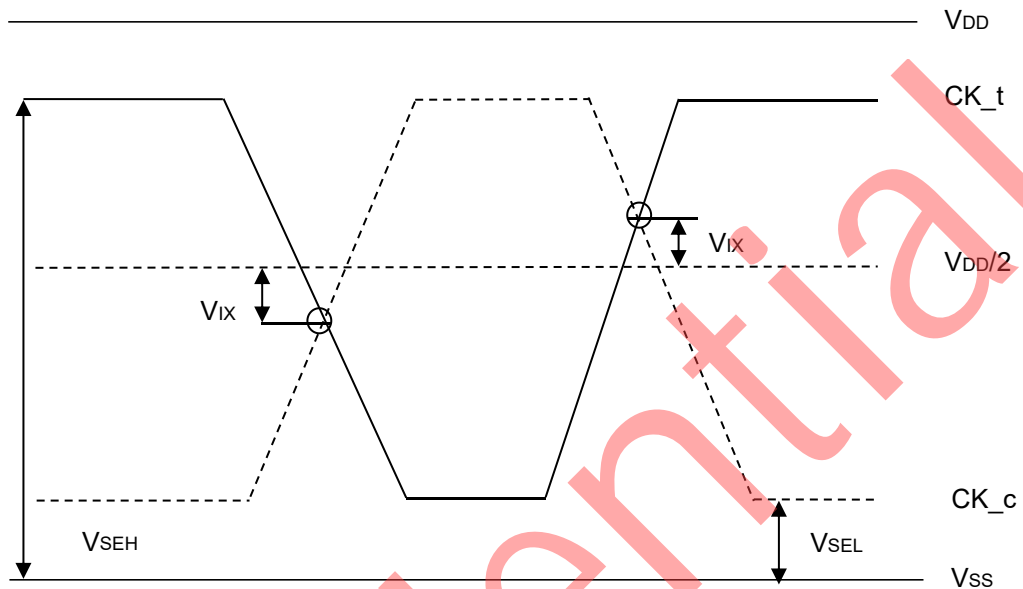


Figure 9 - VIX Definition (CK)

Table 35 - Cross Point Voltage for Differential Input Signals (CK)

Parameter	Symbol	Input Level	DDR4-2400,2666,2933,3200	
			Min	Max
Differential input cross point voltage relative to $V_{DD}/2$ for CK_t, CK_c	$V_{IX}(CK)$	$V_{SEH} > V_{DD}/2 + 135mV$	-	110mV
		$V_{DD}/2 + 90mV \leq V_{SEH} \leq V_{DD}/2 + 135mV$	-	$(V_{SEH} - V_{DD}/2) - 30mV$
		$V_{DD}/2 - 135mV \leq V_{SEL} \leq V_{DD}/2 - 90mV$	$-(V_{DD}/2 - V_{SEL}) + 30mV$	-
		$V_{SEL} \leq V_{DD}/2 - 135mV$	-110mV	-

## 11.6 CMOS Rail to Rail Input Levels

### 11.6.1 CMOS Rail to Rail Input Levels for RESET\_n

Table 36 - CMOS rail to rail Input Levels for RESET\_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

**Note:**

1. After RESET\_n is registered LOW, RESET\_n level shall be maintained below VIL(DC)\_RESET during tPW\_RESET, otherwise, SDRAM may not be reset
2. Once RESET\_n is registered HIGH, RESET\_n level must be maintained above VIH(DC)\_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET\_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal(ringback) requirement during its level transition from Low to High.
5. This definition is applied only "Reset Procedure at Power Stable".
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

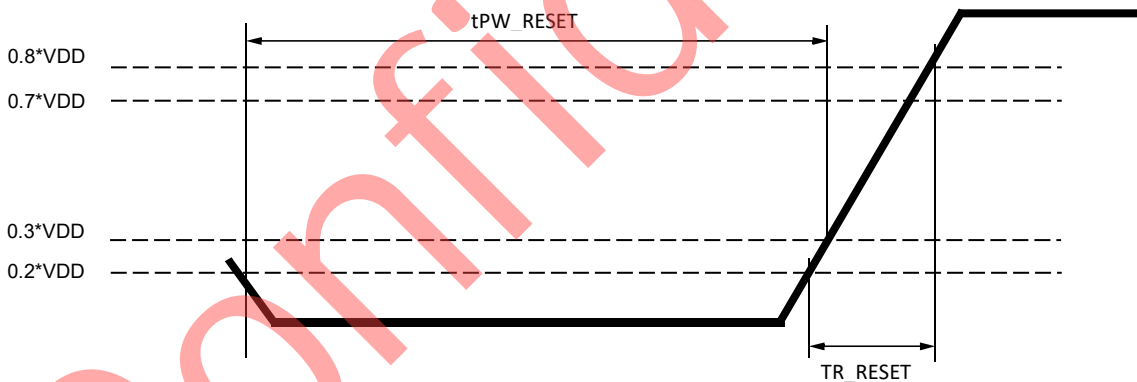


Figure 10 - RESET\_n Input Slew Rate Definition

## 11.7 AC and DC Logic Input Levels for DQS Singals

### 11.7.1 Differential signal definition

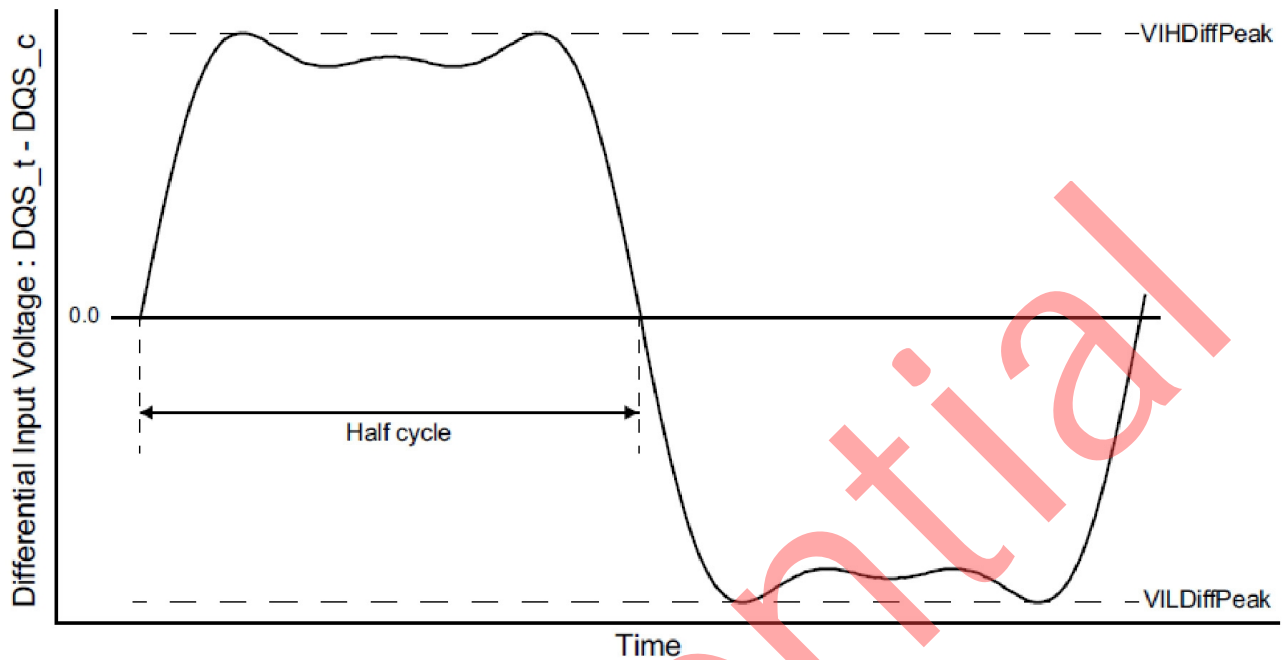


Figure 11 - Definition of differential DQS Signal AC-swing Level

### 11.7.2 Differential swing requirements for DQS (DQS\_t – DQS\_c)

Table 37 – Differential AC and DC Input Levels for DQS

Symbol	Parameter	2400		2666		2933		3200		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	160	Note2	150	VDDQ	145	VDDQ	140	VDDQ	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-160	VSSQ	-150	VSSQ	-145	VSSQ	-140	mV	1

**Note:**

- Used to define a differential signal slew-rate.
- These values are not defined; however, the differential signals DQS\_t – DQS\_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

### 11.7.3 Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

$$V^{IH}.DIFF.Peak\ Voltage = \text{Max}(f(t))$$

$$V^{IL}.DIFF.Peak\ Voltage = \text{Min}(f(t))$$

$$f(t) = VDQS\_t - VDQS\_c$$

The  $\text{Max}(f(t))$  or  $\text{Min}(f(t))$  used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all ui's.

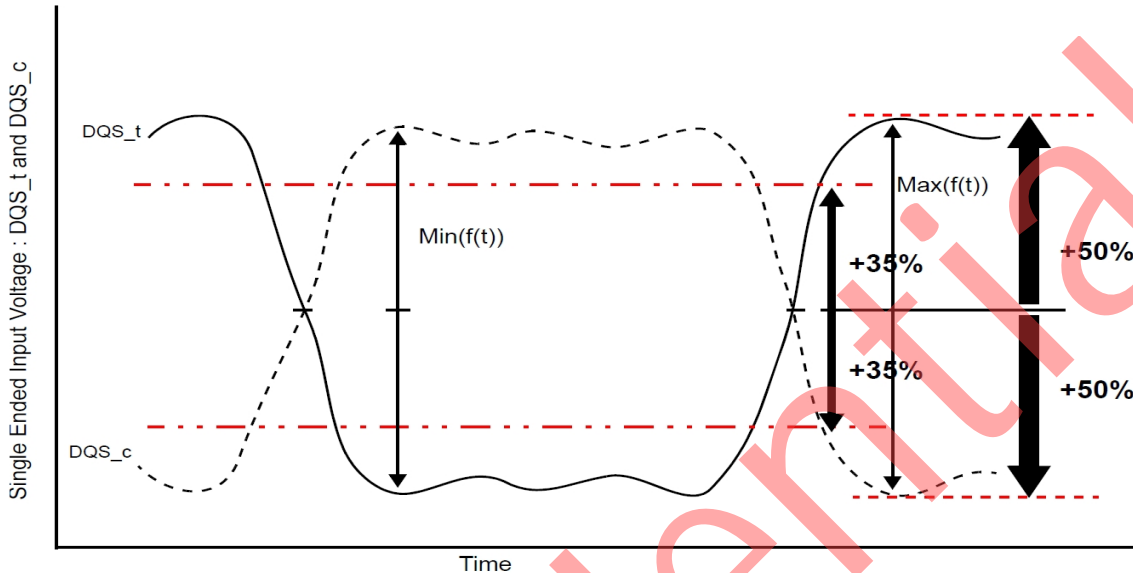


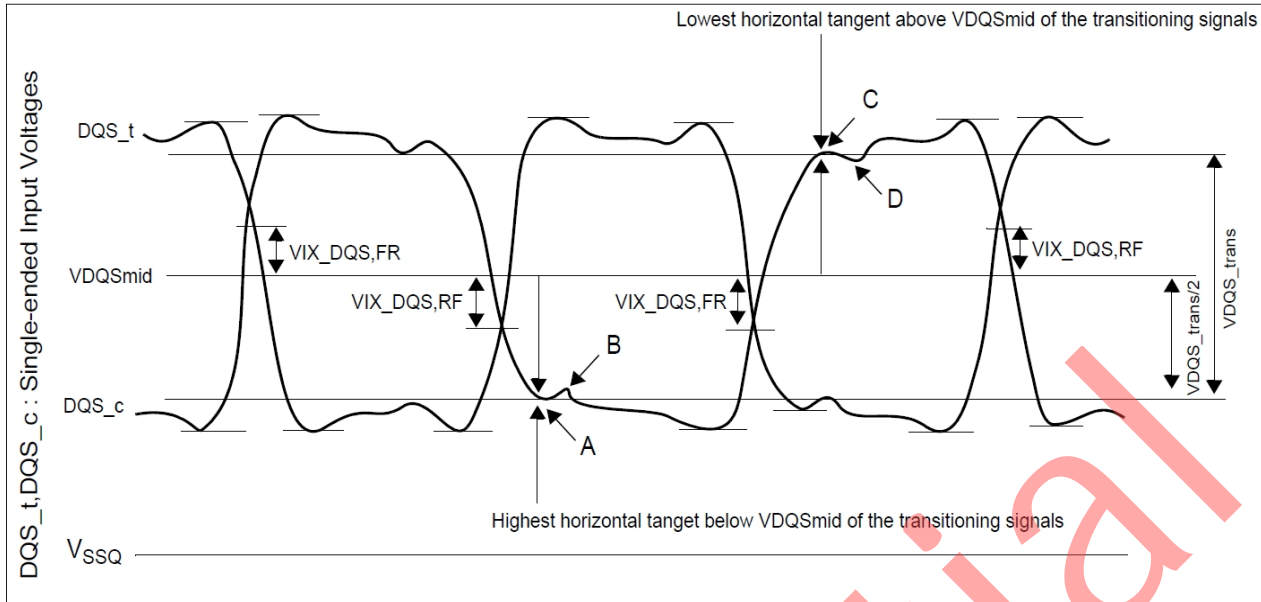
Figure 12 – Definition of differential DQS Peak Voltage and rage of exempt nonmonotonic signaling

### 11.7.4 Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS\_t, DQS\_c) must meet the requirements in Table 38. The differential input cross point voltage VIX\_DQS (VIX\_DQS\_FR and VIX\_DQS\_RF) is measured from the actual cross point of DQS\_t, DQS\_c relative to the VDQSmid of the DQS\_t and DQS\_c signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS\_t and DQS\_c signals, and noted by VDQS\_trans. VDQS\_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS\_t rising) or VIL.DIFF.Peak Voltage (DQS\_c rising), refer to Figure 12. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure 13) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure 13) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure 13) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure 13) is not a valid horizontal tangent.



**Figure 13 —Vix Definition (DQS)**

**Table 38 – Cross point voltage for DQS differential input signals**

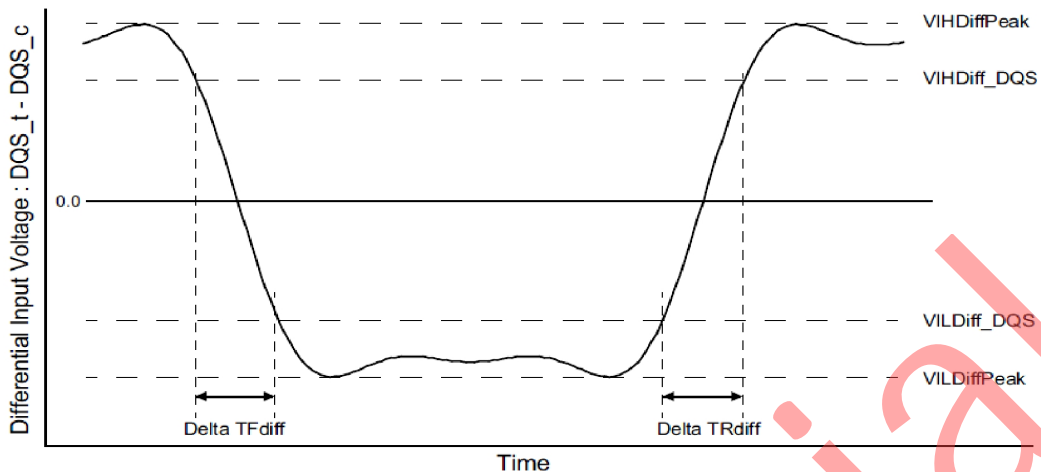
Symbol	Parameter	2400,2666,2933,3200		Unit	Note
		Min	Max		
Vix_DQS_ratio	DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	-	25	%	1,2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	Min(VIHdiff, 50)	mV	3,4,5

**Note:**

1. Vix\_DQS\_Ratio is DQS VIX crossing (Vix\_DQS\_FR or Vix\_DQS\_RF) divided by VDQS\_trans. VDQS\_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2. VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQS drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.
4. Vix measurements are only applicable for transitioning DQS\_t and DQS\_c signals when toggling data, preamble and high-z states are not applicable conditions.
5. The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

## 11.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS\_t, DQS\_c) are defined and measured as shown in Figure 13 and Figure 14.



**Note:**

1. Differential signal rising edge from VILDiff\_DQS to VIHDiff\_DQS must be monotonic slope.
2. Differential signal falling edge from VIHDiff\_DQS to VILDiff\_DQS must be monotonic slope.

**Figure 14 – Differential Input Slew Rate Definition for DQS\_t, DQS\_c**

**Table 39 – Differential Input Slew Rate Definition for DQS\_t, DQS\_c**

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge(DQS_t – DQS_c)	VILDiff_DQS	VIHDiff_DQS	$ VILDiff\_DQS - VIHDiff\_DQS /DeltaTRdiff$
Differential input slew rate for falling edge(DQS_t – DQS_c)	VIHDiff_DQS	VILDiff_DQS	$ VILDiff\_DQS - VIHDiff\_DQS /DeltaTFdiff$

**Table 40 – Differential Input Level for DQS\_t, DQS\_c**

Symbol	Parameter	2400		2666		2933		3200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
VIHDiff_DQS	Differential Input High	130	-	120	-	115	-	110	-	mV
VILDiff_DQS	Differential Input Low	-	-130	-	-120	-	-115	-	-110	mV

**Table 41 – Differential Input Slew Rate for DQS\_t, DQS\_c**

Symbol	Parameter	2400/2666/2933/3200		Unit
		Min	Max	
SRIdiff	Differential Input Slew Rate	3	18	V/ns

## 12 AC and DC output Measurement levels

### 12.1 Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong (low Ron) and weak mode (high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON<sub>Pu</sub> and RON<sub>Pd</sub>) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - V_{out}}{|I_{out}|} \quad \text{under the condition that } RON_{Pd} \text{ is off}$$

$$RON_{Pd} = \frac{V_{out}}{|I_{out}|} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$

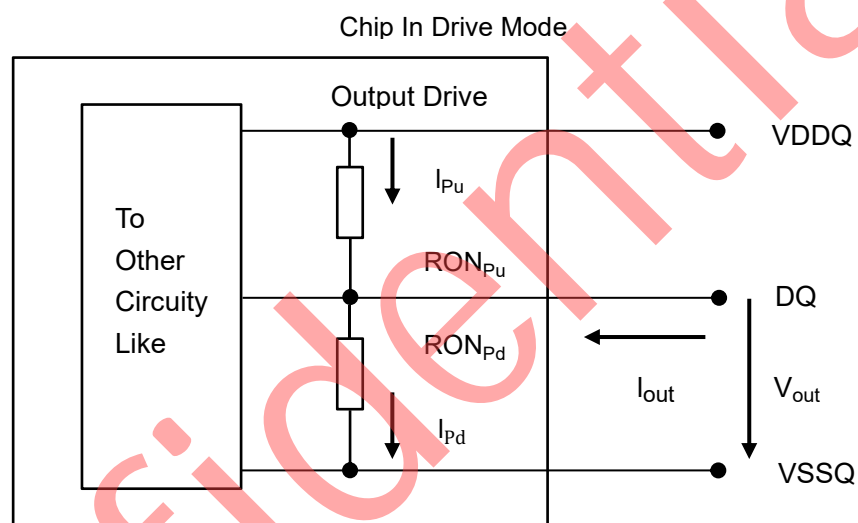


Figure 15 – Output driver

**Table 42 – Output Driver DC Electrical Characteristics, assuming RZQ=240ohm; entire operating temperature range; after proper ZQ calibration.**

RON <sub>NOM</sub>	Resistor	Vout	Min	Nom	Max	Unit	Note
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5*VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
<b>Mismatch between pull-up and pull-down, MMPuPd</b>		VOMdc= 0.8* VDDQ	-10	-	10	%	1,2,3,4
<b>Mismatch DQ-DQ within byte variation pull-up, MMPudd</b>		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
<b>Mismatch DQ-DQ within byte variation pull-dn, MMPddd</b>		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

**Note:**

- The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
- Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 \* VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 \* VDDQ and 1.1 \* VDDQ.
- Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8\*VDD separately; Ronnom is the nominal Ron value.

$$MMP_{uPd} = \frac{RONP_u - RONP_d}{RONNOM} * 100$$

- RON variance range ratio to RON Nominal value in a given component, including DQS\_t and DQS\_c

$$MMP_{udd} = \frac{RONP_uMAX - RONP_uMIN}{RONNOM} * 100$$

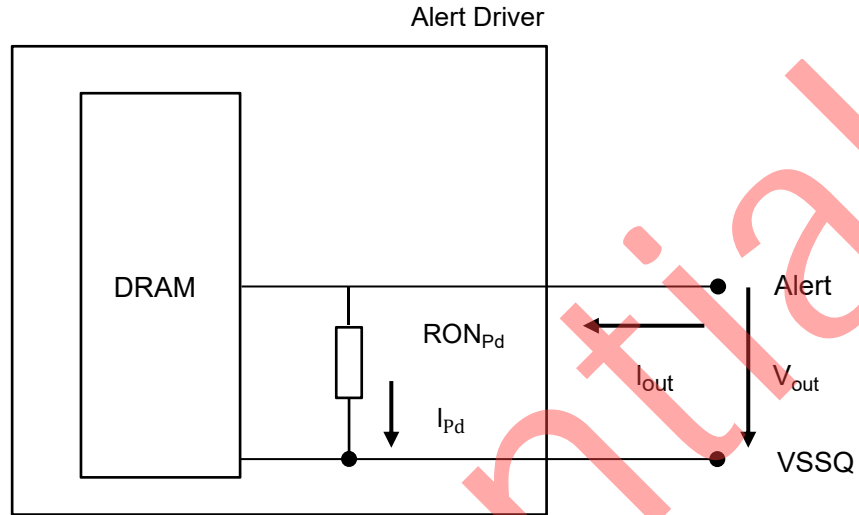
$$MMP_{ddd} = \frac{RONP_dMAX - RONP_dMIN}{RONNOM} * 100$$

- This parameter of x16 device is specified for Upper byte and Lower byte.

## 12.1.1 Alert\_n Output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance  $R_{ON}$  is defined as follows:

$$R_{ON_{Pd}} = \frac{V_{out}}{|I_{out}|} \text{ under the condition that } R_{ON_{Pu}} \text{ is off}$$



Resistor	Vout	Min	Max	Unit	Note
$R_{ON_{Pd}}$	$V_{OLdc} = 0.1 * VDDQ$	0.3	1.2	34Ω	1
	$V_{OMdc} = 0.8 * VDDQ$	0.4	1.2	34Ω	1
	$V_{OHdc} = 1.1 * VDDQ$	0.4	1.4	34Ω	1

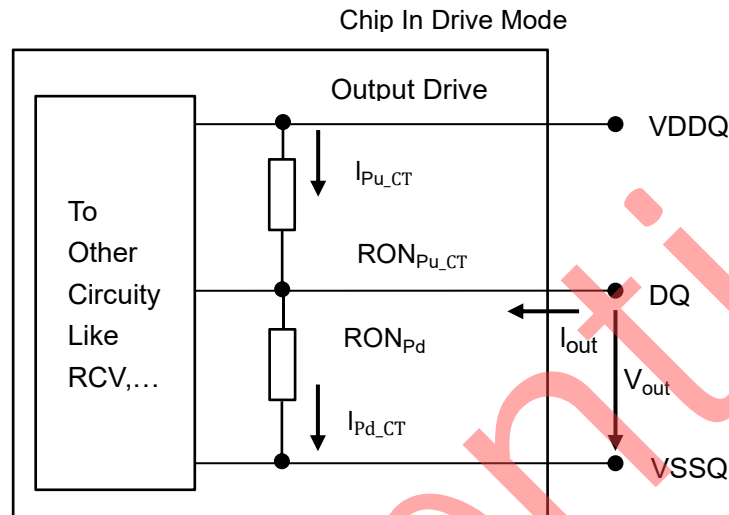
**Note:** VDDQ voltage is at VDDQ DC. VDDQ DC definition is TBD.

## 12.1.2 Output Driver Characteristic of Connectivity Test ( CT ) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode. The individual pull-up and pull-down resistors (RONPu\_CT and RONPd\_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{VDDQ - V_{out}}{|I_{out}|}$$

$$RON_{Pd\_CT} = \frac{V_{out}}{|I_{out}|}$$



RON <sub>NOM_CT</sub>	Resistor	V <sub>out</sub>	Max	Unit	Note
34Ω	RON <sub>Pd_CT</sub>	VOB <sub>dc</sub> = 0.2 x V <sub>DDQ</sub>	1.9	34Ω	1
		VOL <sub>dc</sub> = 0.5 x V <sub>DDQ</sub>	2.0	34Ω	1
		VOM <sub>dc</sub> = 0.8 x V <sub>DDQ</sub>	2.2	34Ω	1
		VOH <sub>dc</sub> = 1.1 x V <sub>DDQ</sub>	2.5	34Ω	1
	RON <sub>Pu_CT</sub>	VOB <sub>dc</sub> = 0.2 x V <sub>DDQ</sub>	2.5	34Ω	1
		VOL <sub>dc</sub> = 0.5 x V <sub>DDQ</sub>	2.2	34Ω	1
		VOM <sub>dc</sub> = 0.8 x V <sub>DDQ</sub>	2.0	34Ω	1
		VOH <sub>dc</sub> = 1.1 x V <sub>DDQ</sub>	1.9	34Ω	1

**Note:**

- Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

## 12.2 Single-ended AC & DC Output Levels

Table 43 – Single-ended AC & DC output levels

Symbol	Parameter	2400/2666/2933/3200	Unit	Note
$VOH_{(DC)}$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$VOM_{(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$VOL_{(DC)}$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$VOH_{(AC)}$	AC output high measurement level (for output SR)	$(0.7 + 0.15) \times V_{DDQ}$	V	1
$VOL_{(AC)}$	AC output low measurement level (for output SR)	$(0.7 - 0.15) \times V_{DDQ}$	V	1

**Note:**

- The swing of  $\pm 0.15 \times V_{DDQ}$  is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of  $RZQ/7\Omega$  and an effective test load of  $50\Omega$  to  $V_{TT} = V_{DDQ}$

## 12.3 Differential AC & DC Output Levels

Table 44 – Differential AC & DC output levels

Symbol	Parameter	2400/2666/2933/3200	Unit	Note
$VOH_{diff}(AC)$	AC differential output high measurement level (for output SR)	$+0.3 \times V_{DDQ}$	V	1
$VOL_{diff}(AC)$	AC differential output low measurement level (for output SR)	$-0.3 \times V_{DDQ}$	V	1

**Note:**

- The swing of  $\pm 0.3 \times V_{DDQ}$  is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of  $RZQ/7\Omega$  and an effective test load of  $50\Omega$  to  $V_{TT} = V_{DDQ}$  at each of the differential outputs.

## 12.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $VOL(AC)$  and  $VOH(AC)$  for single ended signals as shown in Table 45 and Figure 16.

Table 45 – Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$VOL(AC)$	$VOH(AC)$	$[VOH(AC)-VOL(AC)] / \Delta t_{Trse}$
Single ended output slew rate for falling edge	$VOH(AC)$	$VOL(AC)$	$[VOH(AC)-VOL(AC)] / \Delta t_{Tfse}$

**Note:** Output slew rate is verified by design and characterization, and may not be subject to production test.

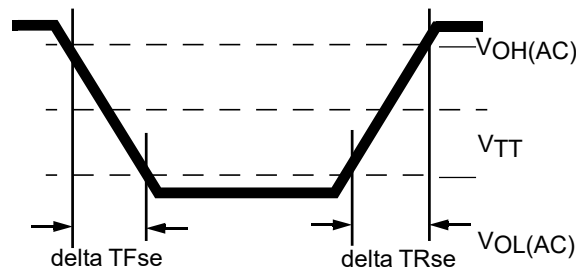


Figure 16 – Single-ended Output Slew Rate Definition

**Table 46 – Single-ended Output Slew Rate**

Parameter	Symbol	2400/2666/2933/3200		Unit
		Min	Max	
Single ended output slew rate	SRQse	4	9	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

**Note:**

- In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
  - Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
  - Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

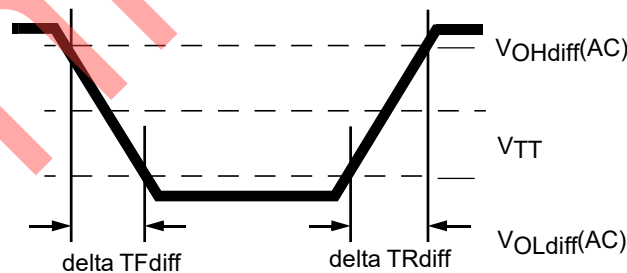
## 12.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 47 and Figure 17.

**Table 47 – Differential Output Slew Rate Definition**

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOHdiff(AC)	VOLdiff(AC)	$[VOHdiff(AC)-VOLdiff(AC)] / \Delta T_{rdiff}$
Differential output slew rate for falling edge	VOLdiff(AC)	VOHdiff(AC)	$[VOHdiff(AC)-VOLdiff(AC)] / \Delta T_{fdiff}$

**Note:** Output slew rate is verified by design and characterization, and may not be subject to production test.



**Figure 17 – Differential Output Slew Rate Definition**

**Table 48 – Differential output slew rate**

Parameter	Symbol	2400/2666/2933/3200		Unit
		Min	Max	
Differential output slew rate	SRQdiff	8	18	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

## 12.6 Single-ended AC and DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Table 49 – Single-ended AC & DC output levels of Connectivity Test Mode

Symbol	Parameter	2400/2666/2933/3200	Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOB(DC)	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
VOL(AC)	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

Note:1. The effective test load is 50Ω terminated by VTT = 0.5\*VDDQ.

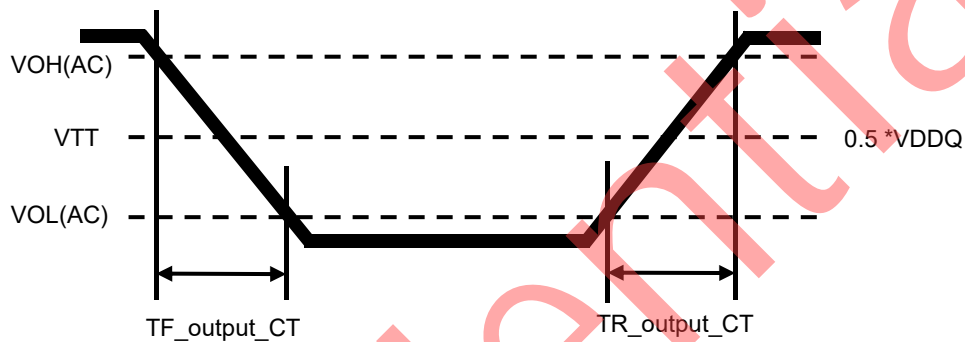


Figure 18 — Output Slew Rate Definition of Connectivity Test Mode

Table 50 – Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	2400/2666/2933/3200		Unit	Note
		Min	Max		
Output signal Falling time	TF_output_CT		10	ns/V	
Output signal Rising time	TR_output_CT		10	ns/V	

## 12.7 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 19.

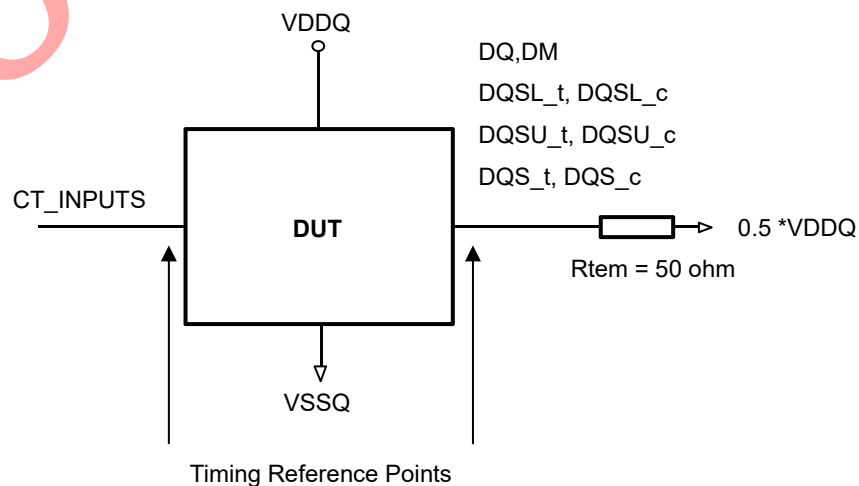


Figure 19 – Connectivity Test Mode Timing Reference Load

## 13 Speed Bin

**Table 51 – DDR4-1600 Speed Bins and Operation**

Speed Bin			DDR4-1600		Unit	NOTE
CL-nRCD-nRP			11-11-11			
Parameter	Symbol		Min	Max		
Internal read command to first data	tAA		13.75 <sup>14</sup> (13.50) <sup>5,12</sup>	18.00	ns	11
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) + 2nCK	ns	11
ACT to internal read or write delay time	tRCD		13.75 (13.50) <sup>5,12</sup>	15.00	ns	11
PRE command period	tRP		13.75 (13.50) <sup>5,12</sup>	15.00	ns	11
ACT to PRE command period	tRAS		35	9 x tREFI	ns	11
ACT to ACT or REF command period	tRC		48.75 (48.50) <sup>5,12</sup>	-	ns	11
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5      1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional) <sup>5,12</sup>	ns	1,2,3,4,11
	CL = 12	CL = 14	tCK(AVG)	1.25	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 14	CL = 16	tCK(AVG)	1.071	ns	1,2,3,6
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 16	CL = 19	tCK(AVG)	0.937	ns	1,2,3,6
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 18	CL = 21	tCK(AVG)	0.833	ns	1,2,3
Supported CL Settings			10, (11), 12,(13),14,(15),16,(17),18		nCK	12
Supported CL Settings with read DBI			12, (13), 14,(15),17,(18),19,(20),21		nCK	
Supported CWL Settings			9, 10, 11, 12 , 14, 16		nCK	

**Table 82 – DDR4-1866 Speed Bins and Operation**

Speed Bin			DDR4-1866		Unit	NOTE
CL-nRCD-nRP			13-13-13			
Parameter	Symbol		Min	Max		
Internal read command to firstdata	tAA		13.92 <sup>14</sup> (13.50) <sup>5,12</sup>	18.00	ns	11
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) + 2nCK	ns	11
ACT to internal read or write delay time	tRCD		13.92 (13.50) <sup>5,12</sup>	15.00	ns	11
PRE command period	tRP		13.92 (13.50) <sup>5,12</sup>	15.00	ns	11
ACT to PRE command period	tRAS		34	9 x tREFI	ns	11
ACT to ACT or REF command period	tRC		47.92 (48.50) <sup>5,12</sup>	-	ns	11
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5      1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25      <1.5 (Optional) <sup>5,12</sup>	ns	1,2,3,4,11
	CL = 12	CL = 14	tCK(AVG)	1.25      <1.5	ns	1,2,3,6
CWL =10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071      <1.25 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 14	CL = 16	tCK(AVG)	1.071      <1.25	ns	1,2,3,6
CWL =11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937      <1.071 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 16	CL = 19	tCK(AVG)	0.937      <1.071	ns	1,2,3,6
CWL =12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833      <0.937 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 18	CL = 21	tCK(AVG)	0.833      <0.937	ns	1,2,3
Supported CL Settings			10, (11), 12,(13),14,(15),16,(17),18		nCK	12
Supported CL Settings with read DBI			12, (13), 14,(15),17,(18),19,(20),21		nCK	
Supported CWL Settings			9, 10, 11, 12 , 14, 16		nCK	

**Table 83 – DDR4-2133 Speed Bins and Operation**

Speed Bin			DDR4-2133		Unit	NOTE
CL-nRCD-nRP			15-15-15			
Parameter	Symbol		Min	Max		
Internal read command to firstdata	tAA		14.06 <sup>14</sup> (13.50) <sup>5,12</sup>	18.00	ns	11
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time	tRCD		14.06 (13.50) <sup>5,12</sup>	15.00	ns	11
PRE command period	tRP		14.06 (13.50) <sup>5,12</sup>	15.00	ns	11
ACT to PRE command period	tRAS		33	9 x tREFI	ns	11
ACT to ACT or REF command period	tRC		47.06 (46.50) <sup>5,12</sup>	-	ns	11
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5      1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25      <1.5 (Optional) <sup>5,12</sup>	ns	1,2,3,4,11
	CL = 12	CL = 14	tCK(AVG)	1.25      <1.5	ns	1,2,3,6
CWL =10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071      <1.25 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 14	CL = 16	tCK(AVG)	1.071      <1.25	ns	1,2,3,6
CWL =11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937      <1.071 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 16	CL = 19	tCK(AVG)	0.937      <1.071	ns	1,2,3,6
CWL =12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833      <0.937 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 18	CL = 21	tCK(AVG)	0.833      <0.937	ns	1,2,3
Supported CL Settings			10, (11), 12,(13),14,(15),16,(17),18		nCK	12
Supported CL Settings with read DBI			12, (13), 14,(15),17,(18),19,(20),21		nCK	
Supported CWL Settings			9, 10, 11, 12 , 14, 16		nCK	

**Table 51 – DDR4-2400 Speed Bins and Operation**

Speed Bin			DDR4-2400		Unit	NOTE
CL-nRCD-nRP			17-17-17			
Parameter	Symbol		Min	Max		
Internal read command to firstdata	tAA		14.16 <sup>14</sup> (13.75) <sup>5,12</sup>	18.00	ns	11
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time	tRCD		14.16 (13.75) <sup>5,12</sup>	-	ns	11
PRE command period	tRP		14.16 (13.75) <sup>5,12</sup>	-	ns	11
ACT to PRE command period	tRAS		32	9 x tREFI	ns	11
ACT to ACT or REF command period	tRC		46.16 (45.75) <sup>5,12</sup>	-	ns	11
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5      1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25      <1.5 (Optional) <sup>5,12</sup>	ns	1,2,3,4,11
	CL = 12	CL = 14	tCK(AVG)	1.25      <1.5	ns	1,2,3,6
CWL =10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071      <1.25 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 14	CL = 16	tCK(AVG)	1.071      <1.25	ns	1,2,3,6
CWL =11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937      <1.071 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 16	CL = 19	tCK(AVG)	0.937      <1.071	ns	1,2,3,6
CWL =12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833      <0.937 (Optional) <sup>5,12</sup>	ns	1,2,3,4,6
	CL = 18	CL = 21	tCK(AVG)	0.833      <0.937	ns	1,2,3
Supported CL Settings			10, (11), 12,(13),14,(15),16,(17),18		nCK	12
Supported CL Settings with read DBI			12, (13), 14,(15),17,(18),19,(20),21		nCK	
Supported CWL Settings			9, 10, 11, 12 , 14, 16		nCK	

**Table 52 – DDR4-2666 Speed Bins and Operation**

Speed Bin			DDR4-2666		Unit	NOTE	
CL-nRCD-nRP			19-19-19				
Parameter	Symbol		Min	Max			
Internal read command to firstdata	tAA		14.25 <sup>14</sup> (13.75) <sup>5,12</sup>	18.00	ns	11	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11	
ACT to internal read or write delay time	tRCD		14.25 (13.75) <sup>5,12</sup>	-	ns	11	
PRE command period	tRP		14.25 (13.75) <sup>5,12</sup>	-	ns	11	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	11	
ACT to ACT or REF command period	tRC		46.25 (45.75) <sup>5,12</sup>	-	ns	11	
	Normal	Read DBI					
<b>CWL = 9</b>	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10
<b>CWL = 9,11</b>	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,11
				(Optional) <sup>5,12</sup>			
<b>CWL = 10,12</b>	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
				(Optional) <sup>5,12</sup>			
<b>CWL = 11,14</b>	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,7
				(Optional) <sup>5,12</sup>			
<b>CWL = 12,16</b>	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,7
				(Optional) <sup>5,12</sup>			
<b>CWL = 14,18</b>	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3
	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3

Speed Bin		DDR4-2666		Unit	NOTE
CL-nRCD-nRP		19-19-19			
Parameter	Symbol	Min	Max		
Supported CL Settings		10, (11), 12,(13),14,(15),16,(17),18,19,20		nCK	12
Supported CL Settings with read DBI		12, (13), 14,(15),17,(18),19,(20),21,22,23		nCK	
Supported CWL Settings		9, 10, 11, 12 , 14, 16,18		nCK	

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**Table 53 – DDR4-2933 Speed Bins and Operation**

Speed Bin			DDR4-2933		Unit	NOTE	
CL-nRCD-nRP			21-21-21				
Parameter	Symbol		Min	Max			
Internal read command to firstdata	tAA		14.32 <sup>14</sup> (13.75) <sup>5,12</sup>	18.00	ns	11	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 4nCK	tAA(max) + 4nCK	ns	11	
ACT to internal read or write delay time	tRCD		14.32 (13.75) <sup>5,12</sup>	-	ns	11	
PRE command period	tRP		14.32 (13.75) <sup>5,12</sup>	-	ns	11	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	11	
ACT to ACT or REF command period	tRC		46.32 (45.75) <sup>5,12</sup>	-	ns	11	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,8,10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,8,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8,12
				(Optional) <sup>5,12</sup>			
CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8,14	
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8,14
				(Optional) <sup>5,12</sup>			
CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8,14	
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8,14
				(Optional) <sup>5,12</sup>			
CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8,14	
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,8,14
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,8,14
				(Optional) <sup>5,12</sup>			
CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,8,14	
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,8,14
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,8,14
				(Optional) <sup>5,12</sup>			
CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,8,14	

Speed Bin			DDR4-2933		Unit	NOTE	
CL-nRCD-nRP			21-21-21				
Parameter		Symbol	Min	Max			
	Normal	Read DBI					
<b>CWL =16,20</b>	CL = 19	CL = 23	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 21	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3,4,8
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3
<b>Supported CL Settings</b>			10, (11), 12,(13),14,(15),16,(17),18,(19),20,21,22		nCK	12	
<b>Supported CL Settings with read DBI</b>			12, (13), 14,(15),16,(18),19,(20),21,(22),23,25,26		nCK	12	
<b>Supported CWL Settings</b>			9, 10, 11, 12 , 14, 15,16,18,20		nCK		

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**Table 54 – DDR4-3200 Speed Bins and Operation**

Speed Bin			DDR4-3200		Unit	NOTE	
CL-nRCD-nRP			22-22-22				
Parameter	Symbol		Min	Max			
Internal read command to firstdata	tAA		13.75	18.00	ns	11	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 4nCK	tAA(max) + 4nCK	ns	11	
ACT to internal read or write delay time	tRCD		13.75	-	ns	11	
PRE command period	tRP		13.75	-	ns	11	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	11	
ACT to ACT or REF command period	tRC		45.75	-	ns	11	
	Normal	Read DBI					
<b>CWL = 9</b>	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,10
<b>CWL = 9,11</b>	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
<b>CWL =10,12</b>	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
<b>CWL =11,14</b>	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
<b>CWL =12,16</b>	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,9
<b>CWL =14,18</b>	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,9
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,9

Speed Bin			DDR4-3200		Unit	NOTE	
CL-nRCD-nRP			22-22-22				
Parameter		Symbol	Min	Max			
	Normal	Read DBI					
CWL =16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.625	<0.75	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.75	ns	1,2,3
Supported CL Settings			10, 11, 12,13,14,15,16,17,18,19,20,21,22,24		nCK	12	
Supported CL Settings with read DBI			12, 13, 14,15,16,18,19,20,21,22,23,24,26,28		nCK		
Supported CWL Settings			9, 10, 11, 12 , 14, 16,18,20		nCK		

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## 13.1 Speed Bin Table Note

### Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
  - VPP = 2.5V +0.25/-0.125 V
  - The values defined with above-mentioned table are DLL ON case
1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
  2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 15.5.
  3. tCK(avg).MAX limits: Calculate  $tCK(avg) = tAA.MAX / CL \text{ SELECTED}$  and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
  4. "Reserved" settings are not allowed. User must program a different value.
  5. "Optional" settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
  6. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
  7. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
  8. Any DDR4-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
  9. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
  10. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
  11. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
  12. CL number in parentheses, it means that these numbers are optional.
  13. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
  14. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

## 14 IDD and IDDQ Specification Parameters and Test Conditions

### 14.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 20 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 21. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as  $V_{IN} \leq V_{ILAC}(\max)$ .
- "1" and "HIGH" is defined as  $V_{IN} \geq V_{IHAC}(\min)$ .
- "MID-LEVEL" is defined as inputs are  $V_{REF} = V_{DD} / 2$ .
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 52.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 53.
  - Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in
  -
- Table 54 through Table 62
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting

RON = RZQ/7 (34 Ohm in MR1);

RTT\_NOM = RZQ/6 (40 Ohm in MR1);

RTT\_WR = RZQ/2 (120 Ohm in MR2);

RTT\_PARK = Disable;

Qoff = 0<sub>B</sub> (Output Buffer enabled) in MR1;

TDQS\_t disabled in MR1;

CRC disabled in MR2;

CA parity feature disabled in MR5;

Read/Write DBI disabled in MR5;

DM disabled in MR5

- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS\_n, ACT\_n, RAS\_n, CAS\_n, WE\_n} = {HIGH, LOW, LOW, LOW, LOW}; apply BG/BA changes when directed.
- Define D# = {CS\_n, ACT\_n, RAS\_n, CAS\_n, WE\_n} = {HIGH, HIGH, HIGH, HIGH, HIGH}; apply invert of BG/BA changes when directed above.

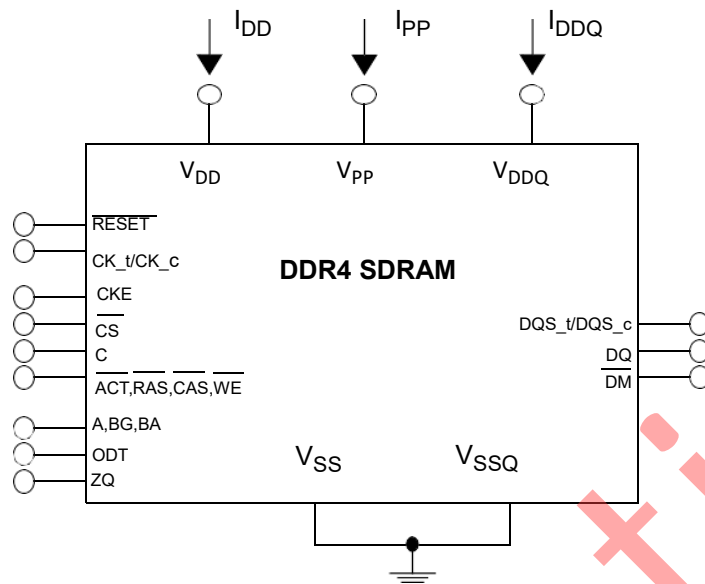


Figure 20 - Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

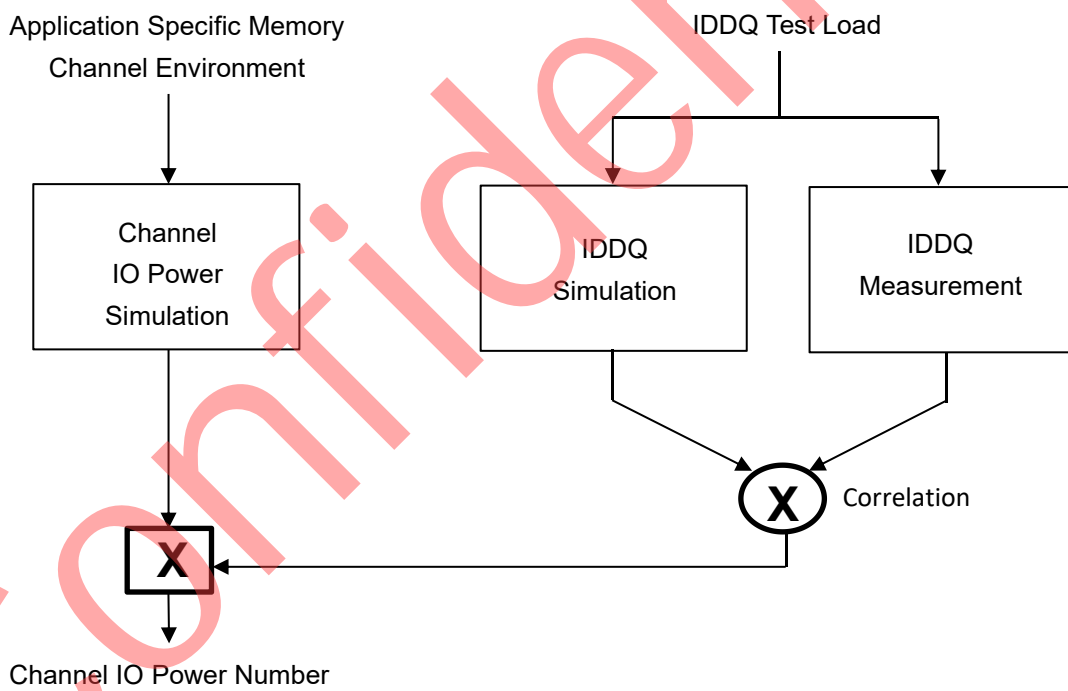


Figure 21 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

Table 52 - Timings Used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
		17-17-17	19-19-19	21-21-21	22-22-22	
tCK		0.833	0.75	0.682	0.625	ns
CL		17	19	21	22	nCK
CWL		14	18	18	20	nCK
nRCD		17	19	21	22	nCK
nRC		56	62	67	74	nCK
nRAS		39	43	47	52	nCK
nRP		17	19	21	22	nCK
nFAW	x4	16	16	16	16	nCK
	x8	26	28	31	34	nCK
	x16	36	40	44	48	nCK
nRRDS	x4	4	4	4	4	nCK
	x8	4	4	4	4	nCK
	x16	7	7	8	9	nCK
nRRDL	x4	6	7	8	8	nCK
	x8	6	7	8	8	nCK
	x16	8	9	10	11	nCK
tCCD_S		4	4	4	4	nCK
tCCD_L		6	7	8	8	nCK
tWTR_S		3	4	4	4	nCK
tWTR_L		9	10	11	12	nCK
nRFC 2Gb		193	214	235	256	nCK
nRFC 4Gb		313	347	382	416	nCK
nRFC 8Gb		421	467	514	560	nCK
TBD						nCK

Table 53 - Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
<b>IDD0</b>	<p>Operating One Bank Active-Precharge Current (AL=0)            CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 52; BL: 8<sup>1</sup>; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to</p> <p>Table 54; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see</p> <p>Table 54 ); Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0; Pattern Details: see</p> <p>Table 54</p>
<b>IDD0A</b>	<p>Operating One Bank Active-Precharge Current (AL=CL-1)            AL = CL-1, Other conditions: see IDD0</p>
<b>IPP0</b>	<p>Operating One Bank Active-Precharge IPP Current            Same condition with IDD0</p>
<b>IDD1</b>	<p>Operating One Bank Active-Read-Precharge Current (AL=0)            CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL : see Table 52; BL: 8<sup>1</sup>; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling according to Table 55; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 55); Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0; Pattern Details: see Table 55.</p>
<b>IDD1A</b>	<p>Operating One Bank Active-Read-Precharge Current (AL=CL-1)            AL = CL-1, Other conditions: see IDD1</p>
<b>IPP1</b>	<p>Operating One Bank Active-Read-Precharge IPP Current            Same condition with IDD1</p>
<b>IDD2N</b>	<p>Precharge Standby Current (AL=0)            CKE: High; External clock: On; tCK, CL: see Table 52 ; BL: 8<sup>1</sup>; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to</p> <p>Table 56; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0; Pattern Details: see</p> <p>Table 56</p>
<b>IDD2NA</b>	<p>Precharge Standby Current (AL=CL-1)            AL = CL-1, Other conditions: see IDD2N</p>
<b>IPP2N</b>	<p>Precharge Standby IPP Current            Same condition with IDD2N</p>
<b>IDD2NT</b>	<p>Precharge Standby ODT Current            CKE: High; External clock: On; tCK, CL: see Table 52 ; BL: 8<sup>1</sup>; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 57; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: toggling according to Table 57; Pattern Details: see Table 57</p>
<b>IDDQ2NT (Optional)</b>	<p>Precharge Standby ODT IDDQ Current            Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current</p>
<b>IDD2NL</b>	<p>Precharge Standby Current with CAL enabled            Same definition like for IDD2N, CAL enabled<sup>3</sup></p>

<b>IDD2NG</b>	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled <sup>3</sup>
<b>IDD2ND</b>	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled <sup>3</sup>
<b>IDD2N_par</b>	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled <sup>3</sup>

Symbol	Description
<b>IDD2P</b>	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL : see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0
<b>IPP2P</b>	Precharge Power-Down IPP Current Same condition with IDD2P
<b>IDD2Q</b>	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0
<b>IDD3N</b>	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 56; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 56
<b>IDD3NA</b>	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N
<b>IPP3N</b>	Active Standby IPP Current Same condition with IDD3N
<b>IDD3P</b>	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0
<b>IPP3P</b>	Active Power-Down IPP Current Same condition with IDD3P
<b>IDD4R</b>	Operating Burst Read Current CKE: High; External clock: On; tCK, CL : see Table 52 ; BL: 8 <sup>2</sup> ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 58; Data IO: seamless read data burst with different data between one burst and the next one according to Table 58 ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 58); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 58
<b>IDD4RA</b>	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R
<b>IDD4RB</b>	Operating Burst Read Current with Read DBI Read DBI enabled <sup>3</sup> , Other conditions: see IDD4R

<b>IPP4R</b>	Operating Burst Read IPP Current Same condition with IDD4R
<b>IDDQ4R</b> <b>(Optional)</b>	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
<b>IDDQ4RB</b> <b>(Optional)</b>	Operating Burst Read IDDQ Current with Read DBI Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current

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Symbol	Description
<b>IDD4W</b>	Operating Burst Write Current CKE: High; External clock: On; tCK, CL : see Table 52 ; BL: 8 <sup>1</sup> ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 59; Data IO: seamless write data burst with different data between one burst and the next one according to Table 59; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 59); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at HIGH; Pattern Details: see Table 59
<b>IDD4WA</b>	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W
<b>IDD4WB</b>	Operating Burst Write Current with Write DBI Write DBI enabled <sup>3</sup> , Other conditions: see IDD4W
<b>IDD4WC</b>	Operating Burst Write Current with Write CRC Write CRC enabled <sup>3</sup> , Other conditions: see IDD4W
<b>IDD4W_par</b>	Operating Burst Write Current with CA Parity CA Parity enabled <sup>3</sup> , Other conditions: see IDD4W
<b>IPP4W</b>	Operating Burst Write IPP Current Same condition with IDD4W
<b>IDD5B</b>	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC : see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 61; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC (see Table 61); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 61
<b>IPP5B</b>	Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B
<b>IDD5F2</b>	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B
<b>IPP5F2</b>	Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2
<b>IDD5F4</b>	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B
<b>IPP5F4</b>	Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F4
<b>IDD6N</b>	Self Refresh Current: Normal Temperature Range: T <sub>CASE</sub> 0 - 85°C; Low Power Auto Self Refresh (LP ASR) : Normal <sup>4</sup> ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
<b>IPP6N</b>	Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N
<b>IDD6E</b>	Self-Refresh Current: Extended Temperature Range) T <sub>CASE</sub> : 0 - 95°C; Low Power Auto Self Refresh (LP ASR) : Extended <sup>4</sup> ; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL

Symbol	Description
<b>IPP6E</b>	Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E
<b>IDD6R</b>	Self-Refresh Current: Reduced Temperature Range $T_{CASE}$ : 0 - 45 °C; Low Power Auto Self Refresh (LP ASR) : Reduced <sup>4</sup> ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
<b>IPP6R</b>	Self Refresh IPP Current: Reduced Temperature Range Same condition with IDD6R
<b>IDD6A</b>	Auto Self-Refresh Current $T_{CASE}$ : 0 - 95°C; Low Power Auto Self Refresh (LP ASR) : Auto <sup>4</sup> ;CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 52; BL: 8 <sup>1</sup> ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
<b>IPP6A</b>	Auto Self-Refresh IPP Current Same condition with IDD6A
<b>IDD7</b>	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL : see Table 52; BL: 8 <sup>1</sup> ; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 62; Data IO: read data bursts with different data between one burst and the next one according to Table 62; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 62; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 62
<b>IPP7</b>	Operating Bank Interleave Read IPP Current Same condition with IDD7
<b>IDD8</b>	Maximum Power Down Current TBD
<b>IPP8</b>	Maximum Power Down IPP Current Same condition with IDD8

**Note:**

- Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
- Output Buffer Enable
  - set MR1 [A12 = 0] : Qoff = Output buffer enabled
  - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
- RTT Nom enable
  - set MR1 [A10:8 = 011] : RTT\_NOM = RZQ/6
- RTT\_WR enable
  - set MR2 [A10:9 = 01] : RTT\_WR = RZQ/2
- RTT\_PARK disable
  - set MR5 [A8:6 = 000]
- CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s  
010] : 1866MT/s, 2133MT/s  
011] : 2400MT/s
- DLL disabled : set MR1 [A0 = 0]
- CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s  
010] : 2400MT/s
- Read DBI enabled : set MR5 [A12 = 1]
- Write DBI enabled : set :MR5 [A11 = 1]
- Low Power Auto Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal; 01] : Reduced Temperature range  
10] : Extended Temperature range; 11] : Auto Self Refresh
- IDD2NG should be measured after sync pulse (NOP) input.

**Table 54 - IDD0, IDD0A and IPP0 Measurement-Loop Pattern<sup>1</sup>**

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3,4	D_#, D_#	1	1	1	1	1	1	0	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																			
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 1 instead																			
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
10	10*nR C	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																					
11	11*nR C	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																					
12	12*nR C	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																					
13	13*nR C	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																					
14	14*nR C	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																					
15	15*nR C	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																					

For x4 and x8 only

**Note:**

1. DQS\_t, DQS\_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

**Table 55 - IDD1, IDD1A and IPP1 Measurement-Loop Pattern<sup>1</sup>**

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3,4	D#, D#	1	1	1	1	1	1	0	0	3 <sup>b</sup>	3	0	0	0	0	7	F	0	-	
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																			
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																			
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	-	
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	1	0	0	3 <sup>b</sup>	3	0	0	0	0	7	F	0	-	
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																			
			1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																			
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		8	7*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		9	9*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
		11	11*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																			
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																			
		13	13*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																			
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																			
15	15*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																					
16	16*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																					

**Note**

1. DQS\_t, DQS\_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

Table 56 - IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N\_par, IPP2,IDD3N, IDD3NA and IDD3P

Measurement-Loop Pattern<sup>1</sup>

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>		
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	0
			3	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 1 instead																		
		2	8-11	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																		
		11	44-47	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																		
		12	48-51	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																		
13	52-55	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																				

**Note:**

1. DQS\_t, DQS\_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

**Table 57 - IDD2NT and IDDQ2NT Measurement-Loop Pattern<sup>1</sup>**

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	0	-
			3	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 1, BA[1:0] = 1 instead																			
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																			
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																			
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																			
13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																					
14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																					
15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																					

For x4 and x8 only

**Note:**

1. DQS\_t, DQS\_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

**Table 58 - IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern<sup>1</sup>**

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2,3	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	-	
		1	4	RD	0	1	1	0	1	0	0	0	1	1	0	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
				5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
				6,7	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		3	12-15	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		4	16-19	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		5	20-23	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		6	24-27	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		7	28-31	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		8	32-35	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		9	36-39	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
		10	40-43	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																			
11	44-47	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																					
12	48-51	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																					
13	52-55	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																					
14	56-59	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																					
15	60-63	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																					

For x4 and x8 only

**Note:**

1. DQS\_t, DQS\_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command.

**Table 59 - IDD4W, IDD4WA, IDD4WB and IDD4W\_par Measurement-Loop Pattern<sup>1</sup>**

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>		
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			1	D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	1	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	0	1	0	1	1	0	0	0	7	F	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	1	0	3 <sup>2</sup>	3	0	0	0	7	F	0	-	
		2	8-11	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																		
11	44-47	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																				
12	48-51	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																				
13	52-55	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																				

**Note:**

1. DQS\_t, DQS\_c are used according to WR Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command..

**Table 60 - IDD4WC Measurement-Loop Pattern<sup>1</sup>**

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC		
			1,2	D, D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-	
			3,4	D#, D#	1	1	1	1	1	1	1	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-	
		1	5	WR	0	1	1	0	0	0	1	0	1	1	0	0	0	7	F	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC	
			6,7	D, D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	1	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-	
		2	10-14	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		3	15-19	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		4	20-24	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		5	25-29	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		6	30-34	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		7	35-39	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		8	40-44	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		9	45-49	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
		10	50-54	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																			
11	55-59	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																					
12	60-64	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																					
13	65-69	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																					
14	70-74	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																					
15	75-79	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																					

**Note:**

1. DQS\_t, DQS\_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command.

**Table 61 - IDD5B Measurement-Loop Pattern<sup>1</sup>**

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>		
Toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		2	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		3	3	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-
		4	4	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-
		4-7	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 1 instead																			
		8-11	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		12-15	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		16-19	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		20-23	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		24-27	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		28-31	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		32-35	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		36-39	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
		40-43	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																			
		44-47	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																			
		48-51	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																			
		52-55	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																			
		56-59	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																			
		60-63	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																			
2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																				

**Note:**

1. DQS\_t, DQS\_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ..

**Table 62 - IDD7 Measurement-Loop Pattern<sup>1</sup>**

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[3,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1	RDA	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3	D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	-	
			...	repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary																			
		1	nRRD	ACT	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-	
			nRRD + 1	RDA	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary-																			
		2	2*nRRD	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		3	3*nRRD	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary																			
		5	nFAW	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		6	nFAW+ nRRD	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		7	nFAW+2*nRRD	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		8	nFAW+3*nRRD	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		9	nFAW+4*nRRD	repeat Sub-Loop 4																			
		10	2*nFAW	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																			
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																			
14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																					
15	3*nFAW	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																					
16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																					
17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																					
18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																					
19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																					
20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																					

**Note:**

1. DQS\_t, DQS\_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

## 14.1 IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

**Table 63 -  $I_{DD}$  and  $I_{DDQ}$  Specification Example**

Parameter	1G x 8				Unit	Note
	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
	17-17-17	19-19-19	21-21-21	22-22-22		
	IDD Max.	IDD Max.	IDD Max.	IDD Max.		
$I_{DD0}$	71	79	84	100	mA	
$I_{DD0A}$	72	80	85	101	mA	
$I_{DD1}$	101	104	114	145	mA	
$I_{DD1A}$	101	104	114	145	mA	
$I_{DD2N}$	50	60	70	81	mA	
$I_{DD2NA}$	51	61	71	82	mA	
$I_{DD2NT}$	85	89	94	99	mA	
$I_{DD2NL}$	50	60	70	81	mA	
$I_{DD2NG}$	49	59	69	80	mA	
$I_{DD2ND}$	40	50	60	70	mA	
$I_{DD2N\_par}$	85	89	94	99	mA	
$I_{DD2P}$	45	50	65	76	mA	
$I_{DD2Q}$	40	50	61	71	mA	
$I_{DD3N}$	81	90	101	112	mA	
$I_{DD3NA}$	82	91	102	113	mA	
$I_{DD3P}$	77	80	92	108	mA	
$I_{DD4R}$	211	231	255	275	mA	
$I_{DD4RA}$	211	231	255	275	mA	
$I_{DD4RB}$	212	232	256	276	mA	
$I_{DD4W}$	178	230	268	285	mA	
$I_{DD4WA}$	178	230	268	285	mA	
$I_{DD4WB}$	178	230	268	285	mA	
$I_{DD4WC}$	190	252	288	305	mA	
$I_{DD4W\_par}$	210	263	298	325	mA	
$I_{DD5B}$	267	299	299	300	mA	
$I_{DD5F2}$	224	224	224	264	mA	
$I_{DD5F4}$	200	200	200	226	mA	
$I_{DD6N}$	25	25	25	25	mA	
$I_{DD6E}$	35	35	35	35	mA	
$I_{DD6R}$	20	20	20	20	mA	
$I_{DD6A}$	22	22	22	22	mA	
$I_{DD7}$	256	268	289	326	mA	
$I_{DD8}$	23	23	23	23	mA	

Parameter	512M x16				Unit	Note
	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
	17-17-17	19-19-19	21-21-21	22-22-22		
	IDD Max.	IDD Max.	IDD Max.	IDD Max.		
$I_{DD0}$	81	89	94	111	mA	
$I_{DD0A}$	82	90	93	112	mA	
$I_{DD1}$	110	114	124	159	mA	
$I_{DD1A}$	111	115	125	160	mA	
$I_{DD2N}$	50	60	70	81	mA	
$I_{DD2NA}$	51	61	71	82	mA	
$I_{DD2NT}$	85	89	94	99	mA	
$I_{DD2NL}$	50	60	70	81	mA	
$I_{DD2NG}$	49	59	69	80	mA	
$I_{DD2ND}$	40	50	60	70	mA	
$I_{DD2N\_par}$	85	89	94	99	mA	
$I_{DD2P}$	45	50	65	76	mA	
$I_{DD2Q}$	40	50	61	71	mA	
$I_{DD3N}$	81	90	101	112	mA	
$I_{DD3NA}$	82	91	102	113	mA	
$I_{DD3P}$	77	80	92	108	mA	
$I_{DD4R}$	271	296	321	359	mA	
$I_{DD4RA}$	275	300	325	365	mA	
$I_{DD4RB}$	271	296	321	359	mA	
$I_{DD4W}$	248	265	280	314	mA	
$I_{DD4WA}$	248	265	280	314	mA	
$I_{DD4WB}$	250	270	281	316	mA	
$I_{DD4WC}$	260	280	291	326	mA	
$I_{DD4W\_par}$	275	295	306	341	mA	
$I_{DD5B}$	267	299	299	300	mA	
$I_{DD5F2}$	224	224	224	264	mA	
$I_{DD5F4}$	200	200	200	226	mA	
$I_{DD6N}$	25	25	25	25	mA	
$I_{DD6E}$	35	35	35	35	mA	
$I_{DD6R}$	20	20	20	20	mA	
$I_{DD6A}$	22	22	22	22	mA	
$I_{DD7}$	358	368	388	420	mA	
$I_{DD8}$	23	23	23	23	mA	

**Table 64 -  $I_{PP}$  Specification Example**

Parameter	1G x 8				Unit	Note
	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
	17-17-17	19-19-19	21-21-21	22-22-22		
	IPP Max.	IPP Max.	IPP Max.	IPP Max.		
$I_{PP0}$	7	7	7	7	mA	
$I_{PP1}$	7	7	7	7	mA	
$I_{PP2N}$	3.5	3.5	3.5	3.5	mA	
$I_{PP2P}$	3.5	3.5	3.5	3.5	mA	
$I_{PP3N}$	4	4	4	4	mA	
$I_{PP3P}$	4	4	4	4	mA	
$I_{PP4R}$	4	4	4	4	mA	
$I_{PP4W}$	4	4	4	4	mA	
$I_{PP5B}$	37	37	37	37	mA	
$I_{PP5B\_F2}$	28	28	28	28	mA	
$I_{PP5B\_F4}$	22	22	22	22	mA	
$I_{PP6N}$	4	4	4	4	mA	
$I_{PP6E}$	4	4	4	4	mA	
$I_{PP7}$	28	28	28	28	mA	
$I_{PP8}$	4	4	4	4	mA	

Parameter	512M x 16				Unit	Note
	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
	17-17-17	19-19-19	21-21-21	22-22-22		
	IPP Max.	IPP Max.	IPP Max.	IPP Max.		
$I_{PP0}$	7	7	7	7	mA	
$I_{PP1}$	7	7	7	7	mA	
$I_{PP2N}$	3.5	3.5	3.5	3.5	mA	
$I_{PP2P}$	3.5	3.5	3.5	3.5	mA	
$I_{PP3N}$	4	4	4	4	mA	
$I_{PP3P}$	4	4	4	4	mA	
$I_{PP4R}$	4	4	4	4	mA	
$I_{PP4W}$	4	4	4	4	mA	
$I_{PP5B}$	37	37	37	37	mA	
$I_{PP5B\_F2}$	28	28	28	28	mA	
$I_{PP5B\_F4}$	22	22	22	22	mA	
$I_{PP6N}$	4	4	4	4	mA	
$I_{PP6E}$	4	4	4	4	mA	
$I_{PP7}$	28	28	28	28	mA	
$I_{PP8}$	4	4	4	4	mA	

**Table 65 -  $I_{DD6}$  Specification**

Parameter	Temperature Range	1G x 8				Unit	Note
		2400	2666	2933	3200		
		17-17-17	19-19-19	21-21-21	22-22-22		
$I_{DD6N}$	0 - 85°C	25	25	25	25	mA	3
$I_{DD6E}$	0 - 95°C	35	35	35	35	mA	4
$I_{DD6R}$	0 - 45°C	20	20	20	20	mA	5
$I_{DD6A}$	0 - 95°C	22	22	22	22	mA	6

Parameter	Temperature Range	512M x 16				Unit	Note
		2400	2666	2933	3200		
		17-17-17	19-19-19	21-21-21	22-22-22		
$I_{DD6N}$	0 - 85°C	25	25	25	25	mA	3
$I_{DD6E}$	0 - 95°C	35	35	35	35	mA	4
$I_{DD6R}$	0 - 45°C	20	20	20	20	mA	5
$I_{DD6A}$	0 - 95°C	22	22	22	22	mA	6

**Note:**

1. Some IDD currents are higher for x16 organization due to larger page-size architecture.
2. Max. values for IDD currents considering worst case conditions of process, temperature and voltage
3. Applicable for MR2 settings A6=0 and A7=0.
4. Applicable for MR2 settings A6=0 and A7=1. IDD6E is only specified for devices which support the Extended Temperature Range feature.
5. Applicable for MR2 settings A6=1 and A7=0. IDD6A is only specified for devices which support the Auto Self Refresh feature.
6. The number of discrete temperature ranges supported and the associated Ta-Tz values are supplier/design specific. Temperature ranges are specified for all supported values of TOPER.
7. Applicable for MR2 settings A6 = 1 and A7=0: Reduced Temperature range. IDD6R is verified by design and characterization, and may not be subject to production test.

## 15 Input/Output Capacitance

Table 66 - Silicon Pad I/O Capacitance

Symbol	Parameter	DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
<b>C<sub>IO</sub></b>	Input/output capacitance	0.55	1.15	0.55	1.15	0.55	1.00	0.55	1.00	pF	1,2,3
<b>C<sub>DIO</sub></b>	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
<b>C<sub>DDQS</sub></b>	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	-	0.05	-	0.05	pF	1,2,3,5
<b>C<sub>CK</sub></b>	Input capacitance, CK_t and CK_c	0.2	0.7	0.2	0.7	0.2	0.7	0.2	0.7	pF	1,3
<b>C<sub>DCK</sub></b>	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	-	0.05	-	0.05	pF	1,3,4
<b>C<sub>I</sub></b>	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.7	0.2	0.7	0.2	0.6	0.2	0.55	pF	1,3,6
<b>C<sub>DI_CTRL</sub></b>	Input capacitance delta(All CTRL pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
<b>C<sub>DI_ADD_CMD</sub></b>	Input capacitance delta(All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
<b>C<sub>ALERT</sub></b>	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
<b>C<sub>ZQ</sub></b>	Input/output capacitance of ZQ	-	2.3	-	2.3	-	2.3	-	2.3	pF	1,3,12
<b>C<sub>TEN</sub></b>	Input capacitance of TEN	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,3,13

**Note:**

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by deembedding the package L and C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBD.
2. DQ, DM\_n, DQS\_T, DQS\_C, TDQS\_T, TDQS\_C. Although the DM, TDQS\_T and TDQS\_C pins have different functions, the loading matches DQ and DQS.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
4. Absolute value CK\_T-CK\_C.
5. Absolute value of CIO(DQS\_T)-CIO(DQS\_C).
6. CI applies to ODT, CS\_n, CKE, A0-A16, BA0-BA1, BG0-BG1, RAS\_n/A16, CAS\_n/A15, WE\_n/A14, ACT\_n and PAR.
7. CDI\_CTRL applies to ODT, CS\_n and CKE.
8.  $CDI\_CTRL = CI(CTRL) - 0.5 * (CI(CLK\_T) + CI(CLK\_C))$ .
9. CDI\_ADD\_CMD applies to, A0-A16, BA0-BA1, BG0-BG1, RAS\_n/A16, CAS\_n/A15, WE\_n/A14, ACT\_n and PAR.
10.  $CDI\_ADD\_CMD = CI(ADD\_CMD) - 0.5 * (CI(CLK\_T) + CI(CLK\_C))$ .
11.  $CDIO = CIO(DQ,DM) - 0.5 * (CIO(DQS\_T) + CIO(DQS\_C))$ .
12. Maximum external load capacitance on ZQ pin: TBD pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

**Table 67 - DRAM Package Electrical Specifications (x8)**

Symbol	Parameter	1Gbx8								Unit	Note
		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200			
		Min	Max	Min	Max	Min	Max	Min	Max		
Z <sub>IO</sub>	Input/output Zpkg	45	85	45	85	48	85	48	85	W	1,2,4,5,10,11
T <sub>dIO</sub>	Input/output Pkg Delay	14	42	14	42	14	40	14	40	ps	1,3,4,5,11
L <sub>IO</sub>	Input/Output Lpkg	-	3.3	-	3.3	-	3.3	-	3.3	nH	11, 12
C <sub>IO</sub>	Input/Output Cpkg	-	0.78	-	0.78	-	0.78	-	0.78	pF	11, 13
Z <sub>IO DQS</sub>	DQS_t, DQS_c Zpkg	45	85	45	85	48	85	48	85	W	1,2,5,10,11
T <sub>dIO DQS</sub>	DQS_t, DQS_c Pkg Delay	14	42	14	42	14	40	14	40	ps	1,3,5,10,11
L <sub>IO DQS</sub>	DQS Lpkg	-	3.3	-	3.3	-	3.3	-	3.3	nH	11, 12
C <sub>IO DQS</sub>	DQS Cpkg	-	0.78	-	0.78	-	0.78	-	0.78	pF	11, 13
DZ <sub>dIO DQS</sub>	Delta Zpkg DQS_t, DQS_c	-	10	-	10	-	10	-	10	W	1,2,5,7,10
DT <sub>dIO DQS</sub>	Delta Delay DQS_t, DQS_c	-	5	-	5	-	5	-	5	ps	1,3,5,7,10
Z <sub>I CTRL</sub>	Input- CTRL pins Zpkg	50	90	50	90	50	90	50	90	W	1,2,5,9,10,11
T <sub>dI CTRL</sub>	Input- CTRL pins Pkg Delay	14	42	14	42	14	40	14	40	ps	1,3,5,9,10,11
L <sub>I CTRL</sub>	Input CTRL Lpkg	-	3.4	-	3.4	-	3.4	-	3.4	nH	11, 12
C <sub>I CTRL</sub>	Input CTRL Cpkg	-	0.7	-	0.7	-	0.7	-	0.7	pF	11, 13
Z <sub>I ADD CMD</sub>	Input- CMD ADD pins Zpkg	50	90	50	90	50	90	50	90	W	1,2,5,8,10,11
T <sub>dI ADD CMD</sub>	Input- CMD ADD pins Pkg Delay	14	45	14	45	14	40	14	40	ps	1,3,5,8,10,11
L <sub>I ADD CMD</sub>	Input CMD ADD Lpkg	-	3.6	-	3.6	-	3.6	-	3.6	nH	11, 12
C <sub>I ADD CMD</sub>	Input CMD ADD Cpkg	-	0.74	-	0.74	-	0.74	-	0.74	pF	11, 13
Z <sub>CK</sub>	CLK_t & CLK_c Zpkg	50	90	50	90	50	90	50	90	W	1,2,5,10,11
T <sub>dCK</sub>	CLK_t & CLK_c Pkg Delay	14	42	14	42	14	42	14	42	ps	1,3,5,10,11
L <sub>i CLK</sub>	Input CLK Lpkg	-	3.4	-	3.4	-	3.4	-	3.4	nH	11, 12
C <sub>i CLK</sub>	Input CLK Cpkg	-	0.7	-	0.7	-	0.7	-	0.7	pF	11, 13
DZ <sub>DCK</sub>	Delta Zpkg CLK_t & CLK_c	-	10	-	10	-	10	-	10	W	1,2,5,6,10
DT <sub>dCK</sub>	Delta Delay CLK_t & CLK_c	-	5	-	5	-	5	-	5	ps	1,3,5,6,10
Z <sub>OZQ</sub>	ZQ Zpkg	-	100	-	100	-	100	-	100	W	1,2,5,10,11
T <sub>dOZQ</sub>	ZQ Delay	20	90	20	90	20	90	20	90	ps	1,3,5,10,11
Z <sub>O ALERT</sub>	ALERT Zpkg	40	100	40	100	40	100	40	100	W	1,2,5,10,11
T <sub>dO ALERT</sub>	ALERT Delay	20	55	20	55	20	55	20	55	ps	1,3,5,10,11

**Note:**

1. This parameter is not subject to production test. It is verified by design and characterization. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side(not pin). Measurement procedure TBD.
2. Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:  $Z_{pkg}(\text{total per pin}) = \sqrt{L_{pkg}/C_{pkg}}$
3. Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:  $T_{d}(\text{total per pin}) = \sqrt{L_{pkg} * C_{pkg}}$
4. Z and Td IO applies to DQ, DM, TDQS\_T and TDQS\_C.
5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
6. Absolute value of ZCK\_t-ZCK\_c for impedance(Z) or absolute value of TdCK\_t-TdCK\_c for delay(Td).
7. Absolute value of ZIO(DQS\_t)-ZIO(DQS\_c) for impedance(Z) or absolute value of TdIO(DQS\_t)-TdIO(DQS\_c) for delay(Td).

8. ZI & Td ADD CMD applies to A0-A13, ACT\_n BA0-BA1, BG0-BG1, RAS\_n/A16 CAS\_n/A15, WE\_n/A14 and PAR.
9. ZI & Td CTRL applies to ODT, CS\_n and CKE.
10. This table applies to monolithic X8 devices.
11. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
12. It is assumed that Lpkg can be approximated as  $L_{pkg} = Z_o * T_d$ .
13. It is assumed that Cpkg can be approximated as  $C_{pkg} = T_d / Z_o$ .

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**Table 68 - DRAM package electrical specifications (X16)**

Symbol	Parameter	512Mx16		Unit	Note
		DDR4-2400 to DDR4-3200			
		Min	Max		
<b>Z<sub>IO</sub></b>	Input/output Zpkg	45	85	W	1
<b>T<sub>dIO</sub></b>	Input/output Pkg Delay	14	45	ps	1
<b>L<sub>IO</sub></b>	Input/Output Lpkg	-	3.4	nH	1,2
<b>C<sub>IO</sub></b>	Input/Output Cpkg	-	0.82	pF	1,3
<b>Z<sub>IO DQS</sub></b>	DQS_t, DQS_c Zpkg	45	85	W	1
<b>T<sub>dIO DQS</sub></b>	DQS_t, DQS_c Pkg Delay	14	45	ps	1
<b>L<sub>IO DQS</sub></b>	DQS Lpkg	-	3.4	nH	1,2
<b>C<sub>IO DQS</sub></b>	DQS Cpkg	-	0.82	pF	1,3
<b>DZ<sub>DIO DQS</sub></b>	Delta Zpkg DQSU_t, DQSU_c	-	10	W	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	W	-
<b>DT<sub>dIO DQS</sub></b>	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	-
<b>Z<sub>I CTRL</sub></b>	Input CTRL pins Zpkg	50	90	W	1
<b>T<sub>dI CTRL</sub></b>	Input CTRL pins Pkg Delay	14	42	ps	1
<b>L<sub>I CTRL</sub></b>	Input CTRL Lpkg	-	3.4	nH	1,2
<b>C<sub>I CTRL</sub></b>	Input CTRL Cpkg	-	0.7	pF	1,3
<b>Z<sub>I ADD CMD</sub></b>	Input- CMD ADD pins Zpkg	50	90	W	1
<b>T<sub>dI ADD CMD</sub></b>	Input- CMD ADD pins Pkg Delay	14	52	ps	1
<b>L<sub>I ADD CMD</sub></b>	Input CMD ADD Lpkg	-	3.9	nH	1,2
<b>C<sub>I ADD CMD</sub></b>	Input CMD ADD Cpkg	-	0.86	pF	1,3
<b>Z<sub>CK</sub></b>	CLK_c Zpkg	50	90	W	1
<b>T<sub>dCK</sub></b>	CLK_c Pkg Delay	14	42	ps	1
<b>L<sub>I CLK</sub></b>	Input CLK Lpkg	-	3.4	nH	1,2
<b>C<sub>I CLK</sub></b>	Input CLK Cpkg	-	0.7	pF	1,3
<b>DZ<sub>DCK</sub></b>	Delta Zpkg CLK_c	-	10	W	-
<b>DT<sub>dCK</sub></b>	Delta Delay CLK_c	-	5	ps	-
<b>Z<sub>OZQ</sub></b>	ZQ Zpkg	-	100	W	-
<b>T<sub>dOZQ</sub></b>	ZQ Delay	20	90	ps	-
<b>Z<sub>O ALERT</sub></b>	ALERT Zpkg	40	100	W	-
<b>T<sub>dO ALERT</sub></b>	ALERT Delay	20	55	ps	-

**Note:**

1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.
2. It is assumed that Lpkg can be approximated as  $L_{pkg} = Z_o * T_d$
3. It is assumed that Cpkg can be approximated as  $C_{pkg} = T_d / Z_o$

## 16 Electrical Characteristics & AC Timing

### 16.1 Reference Load for AC Timing and Output Slew Rate

Figure 22 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

Ron nominal of DQ, DQS\_t and DQS\_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal =  $1.0 * VDDQ$ ,

The minimum DC Low level of Output signal =  $\{ 34 / ( 34 + 50 ) \} * VDDQ = 0.4 * VDDQ$

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low =  $\{ ( 1 + 0.4 ) / 2 \} * VDDQ = 0.7 * VDDQ$

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

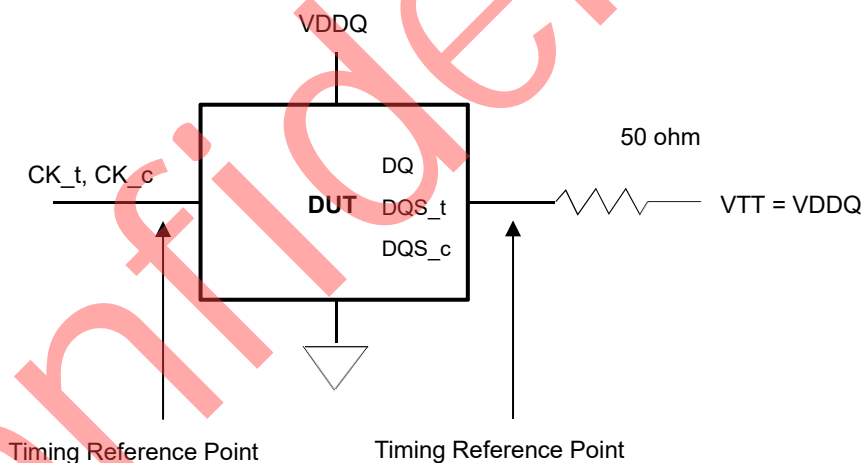


Figure 22 - Reference Load for AC Timing and Output Slew Rate

### 16.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

Table 69 - tREFI by Device Density

Parameter	Symbol	4Gb	8Gb	Unit	Note	
Average periodic refresh interval	tREFI	$0^{\circ}\text{C} \leq \text{TCASE} \leq 85^{\circ}\text{C}$	7.8	7.8	us	
		$-40^{\circ}\text{C} \leq \text{TCASE} \leq 85^{\circ}\text{C}$	7.8	7.8	us	1
		$85^{\circ}\text{C} < \text{TCASE} \leq 95^{\circ}\text{C}$	3.9	3.9	us	

Note: Supported only for Industrial Temperature

## 16.3 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

### 16.3.1 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

### 16.3.2 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left( \sum_{j=1}^N tCK(abs)_j \right) / N \quad N=200$$

### 16.3.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left( \sum_{j=1}^N tCH_j \right) / \{N \times tCK(avg)\} \quad N=200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left( \sum_{j=1}^N tCL_j \right) / \{N \times tCK(avg)\} \quad N=200$$

### 16.3.4 Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

## 16.4 Timing Parameters by Speed Grade

Table 70 - Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Minimum Clock Cycle Time (DLL off mode)	t <sub>CK</sub> (DLL_OFF)	8	20	8	20	8	20	ns	-
Average Clock Period	t <sub>CK</sub> (avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	ns	35,36
Average high pulse width	t <sub>CH</sub> (avg)	0.48	0.52	0.48	0.52	0.48	0.52	t <sub>CK</sub> (avg)	
Average low pulse width	t <sub>CL</sub> (avg)	0.48	0.52	0.48	0.52	0.48	0.52	t <sub>CK</sub> (avg)	
Absolute Clock Period	t <sub>CK</sub> (abs)	Min = t <sub>CK</sub> (avg)min + t <sub>JIT</sub> (per)min_tot Max = t <sub>CK</sub> (avg)max + t <sub>JIT</sub> (per)max_tot						t <sub>CK</sub> (avg)	
Absolute clock HIGH pulse width	t <sub>CH</sub> (abs)	0.45	-	0.45	-	0.45	-	t <sub>CK</sub> (avg)	23
Absolute clock LOW pulse width	t <sub>CL</sub> (abs)	0.45	-	0.45	-	0.45	-	t <sub>CK</sub> (avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	ps	26
Clock Period Jitter during DLL locking period	t <sub>JIT</sub> (per, lck)	-50	50	-43	43	-38	38	ps	
Cycle to Cycle Period Jitter	t <sub>JIT</sub> (cc)	-	125	-	107	-	94	ps	
Cycle to Cycle Period Jitter during DLL locking period	t <sub>JIT</sub> (cc, lck)	-	100	-	86	-	75	ps	
Cumulative error across 2 cycles	t <sub>ERR</sub> (2per)	-92	92	-79	79	-69	69	ps	
Cumulative error across 3 cycles	t <sub>ERR</sub> (3per)	-109	109	-94	94	-82	82	ps	
Cumulative error across 4 cycles	t <sub>ERR</sub> (4per)	-121	121	-104	104	-91	91	ps	
Cumulative error across 5 cycles	t <sub>ERR</sub> (5per)	-131	131	-112	112	-98	98	ps	
Cumulative error across 6 cycles	t <sub>ERR</sub> (6per)	-139	139	-119	119	-104	104	ps	
Cumulative error across 7 cycles	t <sub>ERR</sub> (7per)	-145	145	-124	124	-109	109	ps	
Cumulative error across 8 cycles	t <sub>ERR</sub> (8per)	-151	151	-129	129	-113	113	ps	
Cumulative error across 9 cycles	t <sub>ERR</sub> (9per)	-156	156	-134	134	-117	117	ps	
Cumulative error across 10 cycles	t <sub>ERR</sub> (10per)	-160	160	-137	137	-120	120	ps	
Cumulative error across 11 cycles	t <sub>ERR</sub> (11per)	-164	164	-141	141	-123	123	ps	
Cumulative error across 12 cycles	t <sub>ERR</sub> (12per)	-168	168	-144	144	-126	126	ps	
Cumulative error across 13 cycles	t <sub>ERR</sub> (13per)	-172	172	-147	147	-129	129	ps	
Cumulative error across 14 cycles	t <sub>ERR</sub> (14per)	-175	175	-150	150	-131	131	ps	
Cumulative error across 15 cycles	t <sub>ERR</sub> (15per)	-178	178	-152	152	-133	133	ps	
Cumulative error across 16 cycles	t <sub>ERR</sub> (16per)	-180	180	-155	155	-135	135	ps	
Cumulative error across 17 cycles	t <sub>ERR</sub> (17per)	-183	183	-157	157	-137	137	ps	
Cumulative error across 18 cycles	t <sub>ERR</sub> (18per)	-185	185	-159	159	-139	139	ps	
Cumulative error across n = 13, 14 . . . 49, 50cycles	t <sub>ERR</sub> (nper)	t <sub>ERR</sub> (nper)min = ((1 + 0.68ln(n)) * t <sub>JIT</sub> (per)_total min) t <sub>ERR</sub> (nper)max = ((1 + 0.68ln(n)) * t <sub>JIT</sub> (per)_total max)						ps	
Command and Address setup time to CK_t,CK_c referenced to Vih(ac) / Vil(ac) levels	t <sub>IS</sub> (base)	115	-	100	-	80	-	ps	
Command and Address setup time to CK_t,CK_c referenced to Vref levels	t <sub>IS</sub> (Vref)	215	-	200	-	180	-	ps	
Command and Address hold time to CK_t,CK_c referenced to Vih(dc) / Vil(dc) levels	t <sub>IH</sub> (base)	140	-	125	-	105	-	ps	
Command and Address hold time to CK_t,CK_c referenced to Vref levels	t <sub>IH</sub> (Vref)	215	-	200	-	180	-	ps	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	ps	
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 6.250ns)	-	Max(5nCK, 6.250ns)	-	Max(5nCK, 6.250ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK, 5ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 3.7ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2 K)	Max(4nCK, 5ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 3.7ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 7.5ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 35ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 25ns)	-	Max(20nCK, 23ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 20ns)	-	Max(16nCK, 17ns)	-	Max(16nCK, 15ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	ns	1,2,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	ns	1,34
Internal READ Command to PRECHARGE Command delay	tRTP	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	ns	34
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(4nCK, 3.75ns)	-	tWR+max(5nCK, 3.75ns)	-	tWR+max(5nCK, 3.75ns)	-	ns	1,28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max(4nCK, 3.75ns)	-	tWTR_S+max(5nCK, 3.75ns)	-	tWTR_S+max(5nCK, 3.75ns)	-	ns	2, 29,34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max(4nCK, 3.75ns)	-	tWTR_L+max(4nCK, 3.75ns)	-	tWTR_L+max(5nCK, 3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD(min)+AL+PL	-	tMOD(min)+AL+PL	-	tMOD(min)+AL+PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup ( tRP / tCK(avg))						nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency	tCAL	Max(3nCK, 3.748 ns)	-	Max(3nCK, 3.748 ns)	-	Max(3nCK, 3.748ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	tCK(avg)/2	13,18,39,49
DQ output hold time per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	tCK(avg)/2	13,17,18,39,49
Data Valid Window per device per UI: (tQH -tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	UI	17,18,39,49
Data Valid Window , per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	UI	17,18,39,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-360	180	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	ps	39
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	tCK	39,40
DQS_t, DQS_c differential READ Pre-amble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Pre-amble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Pre-amble (2 clock preamble)	tWPRE2	NA	-	NA	-	NA	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	-	-	-	-	-	-	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		370		330		310	ps	37,38,39
Command path disable delay upon MPSM entry	tMPED	Min = tMOD(min) + tCPDED(min)						nCK	
Valid clock requirement after MPSM entry	tCKMPE	Min = tMOD(min) + tCPDED(min)						nCK	
Valid clock requirement before MPSM exit	tCKMPX	Min = tCKSRX (min)						nCK	
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)						nCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	Min = tXMP(min) + tXSDLL(min)						nCK	
CS setup time to CKE	tMPX_S	Min = tIS(min) + tIH(min)						ns	
CS_n HIGH hold time to CKE rising edge	tMPX_HH	Min = tXP						ns	
CS_n LOW hold time to CKE rising edge	tMPX_IH	Min = 12; Max = tXMP-10ns						ns	
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min)+10ns)	-	max(5nCK, tRFC(min)+10ns)	-	max(5nCK, tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to ZQCL, ZQCS and MRS (CL,CWL,WR and RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	Max(5nCK, 10ns)+PL	-	Max(5nCK, 10ns)+PL	-	max(5nCK, 10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	nCK	
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	nCK	
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+ WR+1	-	WL+4+ WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+ (tWR/tCK(avg))	-	WL+2+ (tWR/tCK(avg))	-	WL+2+ (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+ WR+1	-	WL+2+ WR+1	-	WL+2+ WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	nCK	
Parity Latency	PL	4		4		4		nCK	
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
Exit Reset from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR			tXPR				nCK	
CKE High Assert to Gear Down Enable time (T2/CKE)	tXS_GEAR			tXS				nCK	
MRS command to Sync pulse time (T3)	tSYNC_GEAR			tMOD+4CK				nCK	27
Sync pulse to First valid command (T4)	tCMD_GEAR			tMOD				nCK	27
Geardown setup time	tGEAR_setup	-	-	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	2	-	2	-	nCK	
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	ns	34

**Table 71 - Timing Parameters by Speed Bin for DDR4-2666 to DDR4-3200**

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
<b>Clock Timing</b>											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns	-
Average Clock Period	tCK(avg)	0.833	<0.937	0.75	<0.833	0.682	<0.75	0.625	<0.682	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min = tCK(avg)min + tJIT(per)min_tot Max = tCK(avg)max + tJIT(per)max_tot								tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-42	42	-38	38	-34	34	-32	32	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	-19	19	-17	17	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	-30	30	-27	27	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	83	-	75	-	68	-	62	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	67	-	60	-	55	-	50	ps	
Cumulative error across 2 cycles	tERR(2per)	-61	61	-55	55	-50	50	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-73	73	-66	66	-60	60	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-81	81	-73	73	-66	66	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-87	87	-78	78	-71	71	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-92	92	-83	83	-75	75	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-97	97	-87	87	-79	79	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-101	101	-91	91	-83	83	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-104	104	-94	94	-85	85	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-107	107	-96	96	-88	88	-80	80	ps	
Cumulative error across 11 cycles	tERR(11per)	-110	110	-99	99	-90	90	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-112	112	-101	101	-92	92	-84	84	ps	
Cumulative error across 13 cycles	tERR(13per)	-114	114	-103	103	-93	93	-86	86	ps	
Cumulative error across 14 cycles	tERR(14per)	-116	116	-104	104	-95	95	-87	87	ps	
Cumulative error across 15 cycles	tERR(15per)	-118	118	-106	106	-97	97	-89	89	ps	
Cumulative error across 16 cycles	tERR(16per)	-120	120	-108	108	-98	98	-90	90	ps	
Cumulative error across 17 cycles	tERR(17per)	-122	122	-110	110	-100	100	-92	92	ps	
Cumulative error across 18 cycles	tERR(18per)	-124	124	-112	112	-101	101	-93	93	ps	
Cumulative error across n = 13, 14 . . . 49, 50cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)								ps	
Command and Address setup time to CK_t,CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	62	-	55	-	48	-	40	-	ps	
Command and Address setup time to CK_t,CK_c referenced to Vref levels	tIS(Vref)	162	-	145	-	138	-	130	-	ps	
Command and Address hold time to CK_t,CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	80	-	73	-	65	-	ps	
Command and Address hold time to CK_t,CK_c referenced to Vref levels	tIH(Vref)	162	-	145	-	138	-	130	-	ps	

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Control and Address Input pulse width for each input	tIPW	410	-	385	-	365	-	340	-	ps	
<b>Command and Address Timing</b>											
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 5 ns)	-	Max(5nCK, 5 ns)	-	Max(5nCK, 5ns)	-	Max(5nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK, 3.3ns)	-	Max(4nCK, 3ns)	-	Max(4nCK, 2.7ns)	-	Max(4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK, 3.3ns)	-	Max(4nCK, 3ns)	-	Max(4nCK, 2.7ns)	-	Max(4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 13ns)	-	Max(16nCK, 12ns)	-	Max(16nCK, 10.875ns)	-	Max(16nCK, 10ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	ns	1,2,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	ns	1,34
Internal READ Command to PRECHARGE Command delay	tRTP	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	ns	34
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(4nCK,3.75ns)	-	tWR+max(4nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	ns	1,28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max(4nCK,3.75ns)	-	tWTR_S+max(4nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	ns	2, 29,34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max(4nCK,3.75ns)	-	tWTR_L+max(4nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	768	-	854	-	940	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	Max(24nCK,15ns)	-	Max(24nCK,15ns)	-	Max(24nCK,15ns)	-	Max(24nCK,15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD(min)+AL + PL	-	tMOD(min)+AL + PL	-	tMOD(min)+AL + PL	-	tMOD(min)+AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup ( tRP / tCK(avg))								nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
<b>CS_n to Command Address Latency</b>											
CS_n to Command Address Latency	tCAL	Max(3nCK, 3.748 ns)	-	Max(3nCK, 3.748 ns)	-	Max(3nCK, 3.748ns)	-	Max(3nCK, 3.748ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
<b>DRAM Data Timing</b>											
DQS <sub>t</sub> ,DQS <sub>c</sub> to DQ skew, per group, per access	tDQSQ	-	0.17	-	0.18	-	-	-	-	tCK(avg)/2	13,18,39,49
DQ output hold time per group, per access from DQS <sub>t</sub> ,DQS <sub>c</sub>	tQH	0.74	-	0.74	-	-	-	-	-	tCK(avg)/2	13,17,18,39,49
Data Valid Window per device per UI: (tQH -tDQSQ) of each UI on a given DRAM	tDVWd	0.64	-	TBD	-	-	-	-	-	UI	17,18,39,49
Data Valid Window , per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.72	-	0.72	-	-	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK <sub>t</sub> , CK <sub>c</sub>	tLZ(DQ)	-330	175	-310	170	-280	165	-250	160	ps	39
DQ high impedance time from CK <sub>t</sub> , CK <sub>c</sub>	tHZ(DQ)	-	175	-	170	-	165	-	160	ps	39
<b>DRAM Strobe Timing</b>											
DQS <sub>t</sub> , DQS <sub>c</sub> differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	tCK	39,40
DQS <sub>t</sub> , DQS <sub>c</sub> differential READ Pre-amble (2 clock preamble)	tRPRE2	1.8	NOTE44	1.8	NOTE44	1.8	NOTE44	1.8	NOTE44	tCK	39,41
DQS <sub>t</sub> , DQS <sub>c</sub> differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS <sub>t</sub> ,DQS <sub>c</sub> differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS <sub>t</sub> ,DQS <sub>c</sub> differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS <sub>t</sub> , DQS <sub>c</sub> differential WRITE Pre-amble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS <sub>t</sub> , DQS <sub>c</sub> differential WRITE Pre-amble (2 clock preamble)	tWPRE2	1.8	-	1.8	-	1.8	-	1.8	-	tCK	43
DQS <sub>t</sub> , DQS <sub>c</sub> differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS <sub>t</sub> and DQS <sub>c</sub> low-impedance time (Referenced from RL-1)	tLZ(DQS)	-330	175	-310	170	-280	165	-250	160	ps	39
DQS <sub>t</sub> and DQS <sub>c</sub> high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	175	-	170	-	165	-	160	ps	39
DQS <sub>t</sub> , DQS <sub>c</sub> differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS <sub>t</sub> , DQS <sub>c</sub> differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS <sub>t</sub> , DQS <sub>c</sub> rising edge to CK <sub>t</sub> , CK <sub>c</sub> rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS <sub>t</sub> , DQS <sub>c</sub> rising edge to CK <sub>t</sub> , CK <sub>c</sub> rising edge (2 clock preamble)	tDQSS2	-	-	-	-	-	-	-	-	tCK	43
DQS <sub>t</sub> , DQS <sub>c</sub> falling edge setup time to CK <sub>t</sub> , CK <sub>c</sub> rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS <sub>t</sub> , DQS <sub>c</sub> falling edge hold time from CK <sub>t</sub> , CK <sub>c</sub> rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS <sub>t</sub> , DQS <sub>c</sub> rising edge output timing locatino from rising CK <sub>t</sub> , CK <sub>c</sub> with DLL On mode	tDQSCK (DLL On)	-175	175	-170	170	-165	165	-160	160	ps	37,38,39
DQS <sub>t</sub> , DQS <sub>c</sub> rising edge output variance window per DRAM	tDQSCKI (DLL On)		290		270		265		260	ps	37,38,39
<b>MPSM Timing</b>											
Command path disable delay upon MPSM entry	tMPED	Min = tMOD(min) + tCPDED(min)								nCK	
Valid clock requirement after MPSM entry	tCKMPE	Min = tMOD(min) + tCPDED(min)								nCK	
Valid clock requirement before MPSM exit	tCKMPX	Min = tCKSRX (min)								nCK	
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)								nCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	Min = tXMP(min) + tXSDLL(min)								nCK	
CS setup time to CKE	tMPX_S	Min = tIS(min) + tIH(min)								ns	
CS <sub>n</sub> HIGH hold time to CKE rising edge	tMPX_HH	Min = tXP								ns	
CS <sub>n</sub> LOW hold time to CKE rising edge	tMPX_IH	Min = 12; Max = tXMP-10ns								ns	
<b>Calibration Timing</b>											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
<b>Reset/Self Refresh Timing</b>											
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min)+10ns)	-	max(5nCK, tRFC(min)+10ns)	-	max(5nCK, tRFC(min)+10ns)	-	max(5nCK, tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to ZQCL, ZQCS and MRS (CL,CWL,WR and RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	Max(5nCK, 10ns)+PL	-	Max(5nCK, 10ns)+PL	-	max(5nCK, 10ns)+PL	-	max(5nCK, 10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	nCK	
<b>Power Down Timing</b>											
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	nCK	
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+ WR+1	-	WL+4+ WR+1	-	WL+4+WR+1	-	WL+4+ WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+ (tWR/tCK(avg))	-	WL+2+ (tWR/tCK(avg))	-	WL+2+ (tWR/tCK(avg))	-	WL+2+ (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+ WR+1	-	WL+2+ WR+1	-	WL+2+ WR+1	-	WL+2+ WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	
<b>PDA Timing</b>											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		nCK	
<b>ODT Timing</b>											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
<b>Write Leveling Timing</b>											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	
<b>CA Parity Timing</b>											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	72	144	80	160	88	176	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	64	-	71	-	78	-	85	nCK	
Parity Latency	PL	5		5		6		6		nCK	
<b>CRC Error Reporting</b>											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
<b>Geardown timing</b>											
Exit Reset from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	-	-	tXPR				nCK	
CKE High Assert to Gear Down Enable time (T2/CKE)	tXS_GEAR	-	-	-	-	tXS				nCK	
MRS command to Sync pulse time (T3)	tSYNC_GEAR	-	-	-	-	tMOD+4CK				nCK	27
Sync pulse to First valid command (T4)	tCMD_GEAR	-	-	-	-	tMOD				nCK	27
Geardown setup time	tGEAR_setup	-	-	2	-	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	2	-	2	-	2	-	nCK	
<b>tREFI</b>											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	ns	34

**NOTE:**

- Start of internal write transaction is defined as follows :  
For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.  
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.  
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
- A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
- Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
- tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rounding algorithm defined in Section 15.5.

5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports  $t_{nPARAM}[nCK]=RU\{t_{PARAM}[ns]/t_{CK}(avg)[ns]\}$ , which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, tWR\_CRC\_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR\_S\_CRC\_DM is used in place of tWTR\_S.
11. When CRC and DM are both enabled tWTR\_L\_CRC\_DM is used in place of tWTR\_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing. Measurement method TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual  $t_{jit(per)}_{total}$  of the input clock. (output deratings are relative to the SDRAM input clock). Example TBD
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge.
21. tQSH describes the instantaneous differential output high pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks.
28. When CRC and DM are both enabled, tWR\_CRC\_DM is used in place of tWR.
29. When CRC and DM are both enabled, tWTR\_S\_CRC\_DM is used in place of tWTR\_S.
30. When CRC and DM are both enabled, tWTR\_L\_CRC\_DM is used in place of tWTR\_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from  $t_{CK}(avg)_{min}$  to  $t_{CK}(avg)_{max}$  at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables show in selection 11.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.  $UI=t_{CK}(avg)_{min}/2$
37. Applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for  $RZQ/7 RON_{NOM} = 34$  ohms.
40. 1tCK toggle mode with setting MR4:A11 to 0.
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0.
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point.
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High.
47. VrefDQ value must be set to either its midpoint or Vcent\_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately  $0.7 * VDDQ$  as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to  $V_{TT} = VDDQ$ .
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

## 16.5 Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like tAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks.

$$nCK = \text{ceiling} [ (\text{parameter\_in\_ns} / \text{application\_tCK\_in\_ns}) - 0.025 ]$$

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

$$nCK = \text{truncate} [ \{ (\text{parameter\_in\_ps} \times 1000) / (\text{application\_tCK\_in\_ps}) + 974 \} / 1000 ]$$

- Either algorithm yields identical results.

### 16.6 The DQ Input Receiver Compliance Mask for Voltage and Timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal with BER of 1e-16; any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

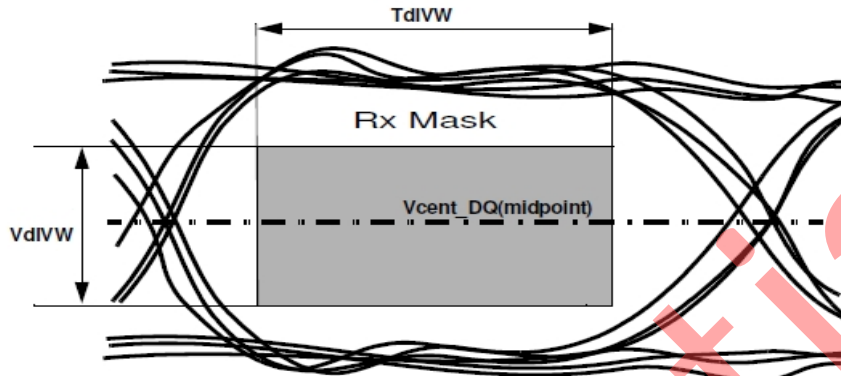


Figure 23 —DQ Receiver(Rx) compliance mask

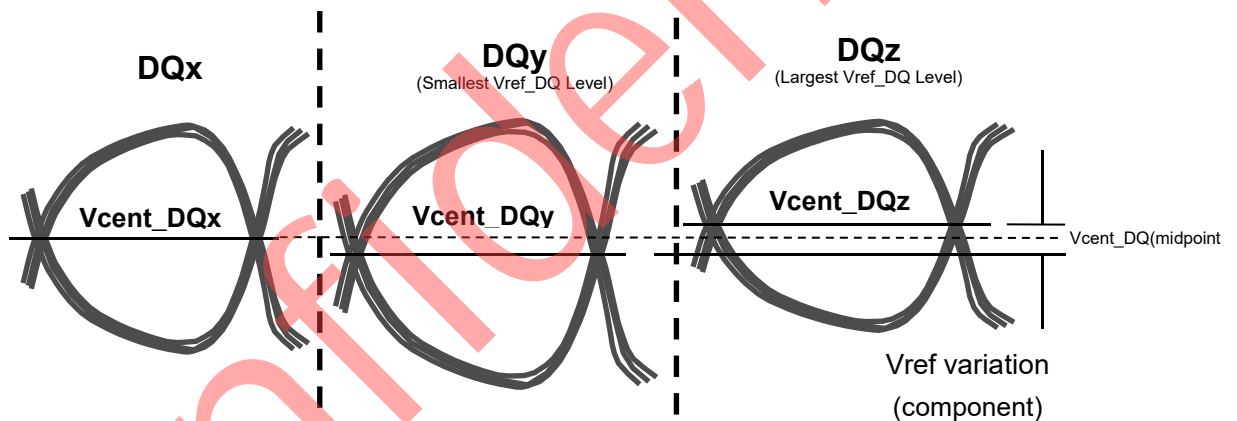
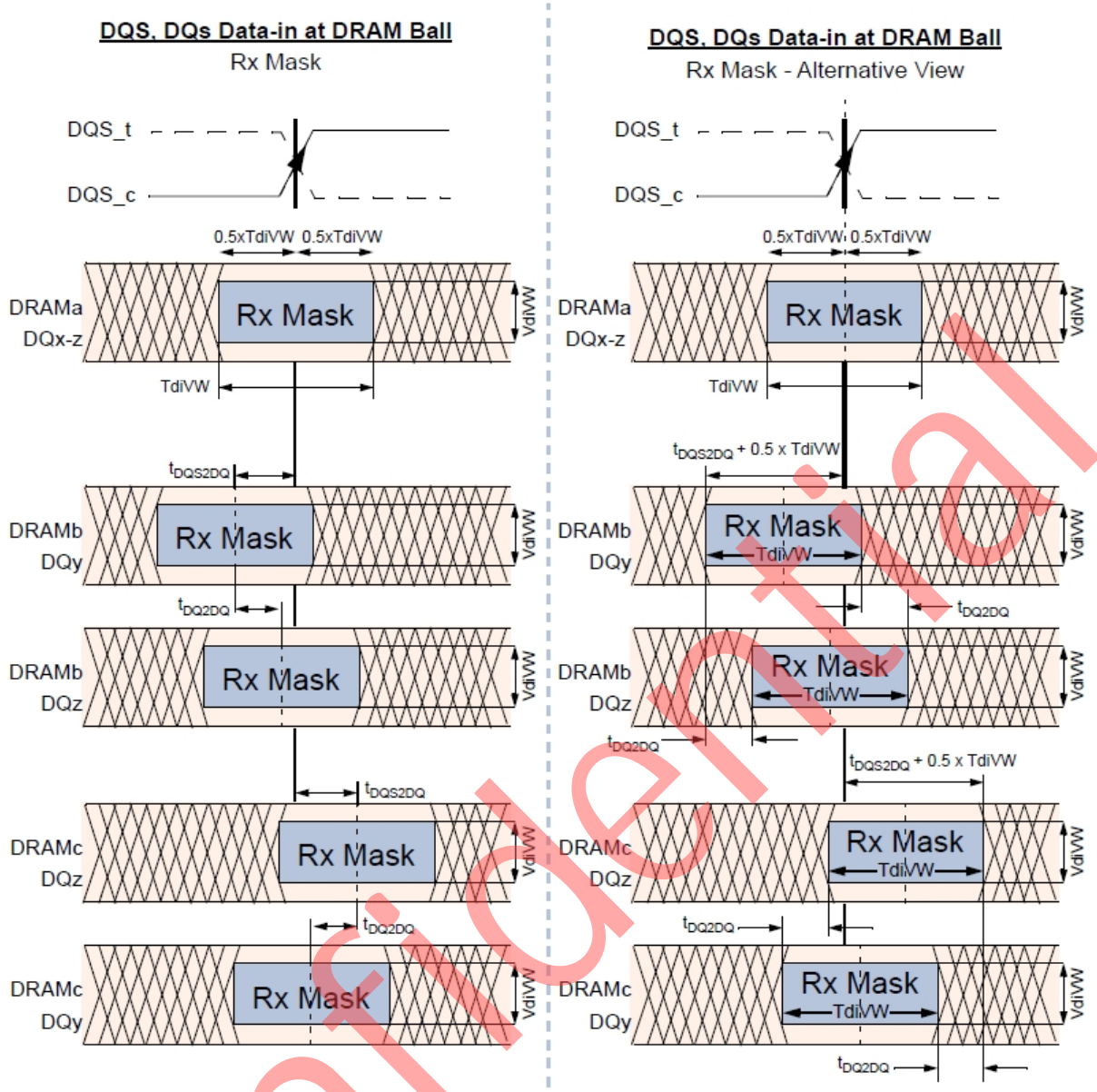


Figure 24 - Vcent\_DQ Variation to Vcent\_DQ(midpoint)

The Vref\_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent\_DQ(midpoint), in order to have valid Rx Mask values.

Vcent\_DQ is defined as the midpoint between the largest Vref\_DQ voltage level and the smallest Vref\_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 24. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.



**NOTE:** DQx represents an optimally centered mask.  
 DQy represents earliest valid mask.  
 DQz represents latest valid mask.

**NOTE :** DRAMa represents a DRAM without any DQS/DQ skews.  
 DRAMB represents a DRAM with early skews (negative  $t_{DQS2DQ}$ ).  
 DRAMc represents a DRAM with delayed skews (positive  $t_{DQS2DQ}$ ).

**NOTE:** Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.  
 $t_{DiPW}$  is not shown; composite data-eyes shown would violate  $t_{DiPW}$ .  
 $V_{CENT DQ}(\text{midpoint})$  is not shown but is assumed to be midpoint of  $V_{diVW}$

**Figure 25 - DQS to DQ and DQ to DQ Timings at DRAM Balls**

All of the timing terms in Figure 25 are measured at the  $V_{diVW}$  levels centered around  $V_{cent\_DQ}(\text{midpoint})$  and are referenced to the  $DQS\_t/DQS\_c$  center aligned to the DQ per pin.

The rising edge slew rates are defined by  $srr1$  and  $srr2$ . The slew rate measurement points for a rising edge are shown in Figure 26 below: A low to high transition  $tr1$  is measured from  $0.5 \cdot V_{diVW}(\text{max})$  below  $V_{cent\_DQ}(\text{midpoint})$  to the last transition through  $0.5 \cdot V_{diVW}(\text{max})$  above  $V_{cent\_DQ}(\text{midpoint})$  while  $tr2$  is measured from the last transition through  $0.5 \cdot V_{diVW}(\text{max})$  above  $V_{cent\_DQ}(\text{midpoint})$  to the first transition through the  $0.5 \cdot V_{IHL\_AC}(\text{min})$  above  $V_{cent\_DQ}(\text{midpoint})$ .

Rising edge slew rate equations:

$$srr1 = VdIVW(max) / tr1$$

$$srr2 = (VIHL\_AC(min) - VdIVW(max)) / (2*tr2)$$

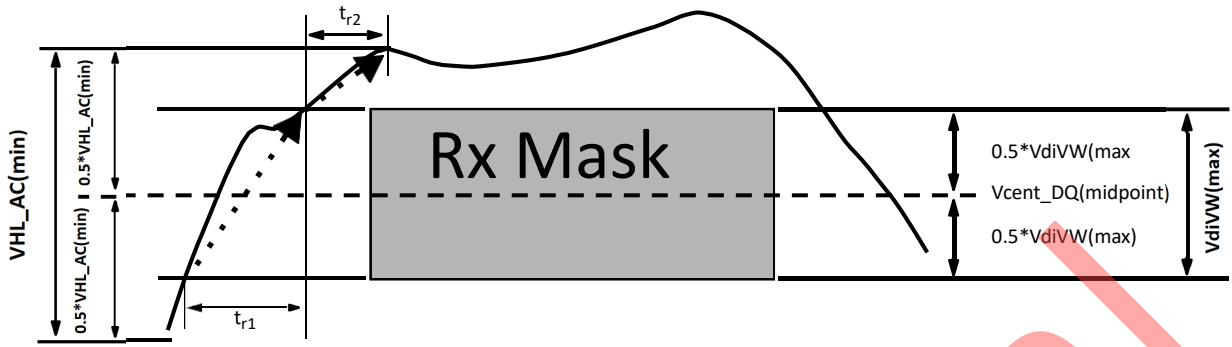


Figure 26 - Slew Rate Conditions For Rising Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure 27 below: A high to low transition tf1 is measured from 0.5\*VdiVW(max) above Vcent\_DQ(midpoint) to the last transition through 0.5\*VdiVW(max) below Vcent\_DQ(midpoint) while tf2 is measured from the last transition through 0.5\*VdiVW(max) below Vcent\_DQ(midpoint) to the first transition through the 0.5\*VIHL\_AC(min) below Vcent\_DQ(pin mid).

Falling edge slew rate equations:

$$srf1 = VdIVW(max) / tf1$$

$$srf2 = (VIHL\_AC(min) - VdIVW(max)) / (2*tf2)$$

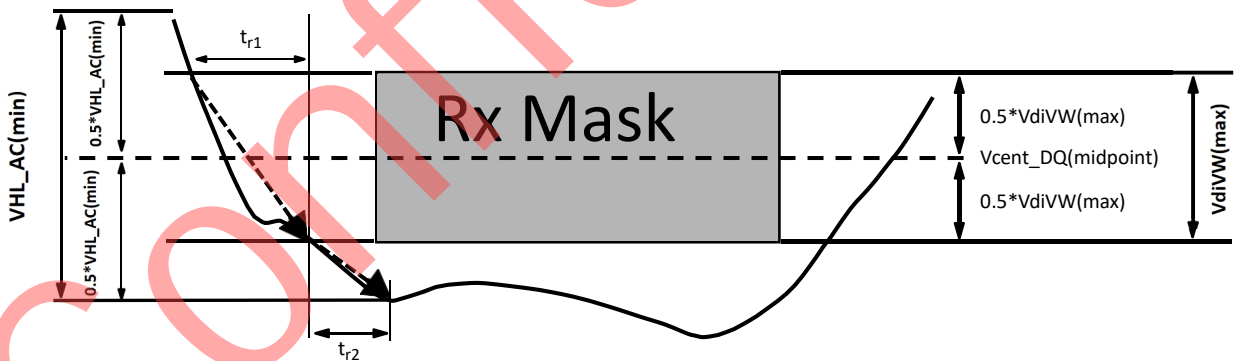


Figure 27 - Slew Rate Conditions For Falling Transition

**Table 72- DRAM DQs In Receive Mode; \* UI=tck(avg)min/2**

Symbol	Parameter	DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
VdIVW	Rx Mask voltage - pk-pk	-	130	-	120	-	115	-	110	mV	1,2,10
TdIVW	Rx timing window	-	0.2	-	0.22	-	0.23	-	0.23	UI*	1,2,10
VIHL_AC	DQ AC input swing pk-pk	160	-	150	-	145	-	140	-	mV	3,4,10
TdIPW	DQ input pulse width	0.58	-	0.58	-	0.58	-	0.58	-	UI*	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.17	0.17	-0.19	0.19	-0.22	0.22	-0.22	0.22	UI*	6, 10
tDQ2DQ	Rx Mask DQ to DQ offset	-	tdb	-	0.105	-	0.115	-	0.125	UI*	7
srr1, srf1	Input Slew Rate over VdIVW if tCK >= 0.935ns	1.0	9	1.0	tdb	1.0	tdb	tdb	tdb	V/ns	8,10
	Input Slew Rate over VdIVW if 0.935ns > tCK >= 0.625ns	1.25	9	1.25	tdb	1.25	tdb	tdb	tdb	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2*srr1	9	0.2*srr1	tdb	0.2*srr1	tdb	tdb	tdb	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2*srf1	9	0.2*srf1	tdb	0.2*srf1	tdb	tdb	tdb	V/ns	9,10

**Note:**

1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent\_DQ (midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = e-16 when the RxMask is not violated. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tdb).
2. Defined over the DQ internal Vref range 1.
3. See Overshoot and Undershoot Specification.
4. DQ input pulse signal swing into the receiver must meet or exceed VIHL AC(min). VIHL\_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e. a valid TdiPW.
5. DQ minimum input pulse width defined at the Vcent\_DQ( midpoint).
6. DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
8. Input slew rate over VdIVW Mask centered at Vcent\_DQ( midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.
9. Input slew rate between VdIVW Mask edge and VIHL\_AC(min) points.
10. All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiW(min), VdiVW(max), and minimum slew rate limits, then either TdiW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

## 16.7 Command, Control and Address Setup, Hold and Derating

The total tIS (setup time) and tIH (hold time) required is calculated to account for slew rate variation by adding the data sheet tIS(base) values, the VIL(AC)/VIH(AC) points, and tIH (base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS (total setup time) = tIS (base) + ΔtIS. For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)min that does not ring back above VIL(DC)max.

**Table 73 – Command, Address, Control Setup and Hold Values**

Symbol	2400	2666	2933	3200	Unit	Reference
tIS(base, AC100)	62	55	48	40	ps	VIH/L(ac)
tIH(base, DC75)	87	80	73	65	ps	VIH/L(dc)
tIS(base, AC tbd)	-	-	-	-	ps	VIH/L(ac)
tIH(base, DC tbd)	-	-	-	-	ps	VIH/L(dc)
tIS/tIH@VREF	162	145	138	130	ps	

Note:

1. Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.
2. Values listed are referenced only; applicable limits are defined elsewhere.

**Table 74 – Command, Address, Control Setup and Hold Values**

Symbol	2400	2666	2933	3200	Unit	Reference
VIH.CA(AC)min	100	90	90	90	mV	VIH/L(ac)
VIH.CA(DC)min	75	65	65	65	mV	VIH/L(dc)
VIL.CA(AC)max	-75	-65	-65	-65	mV	VIH/L(ac)
VIL.CA(DC)max	-100	-90	-90	-90	mV	VIH/L(dc)

Note:

1. Command, Address, Control input levels relative to VREFCA.
2. Values listed are referenced only; applicable limits are defined elsewhere

**Table 75 - Derating value DDR4-2400/2666/2933/3200 tIS/tIH – ac/dc based**

$\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based <sup>1</sup>																	
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$
<b>CMD, ADDR, CNTL Input Slew Rate V/ns</b>	<b>7.0</b>	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	<b>6.0</b>	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	<b>5.0</b>	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	<b>4.0</b>	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	<b>3.0</b>	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	<b>2.0</b>	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	<b>1.5</b>	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	<b>1.0</b>	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	<b>0.9</b>	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	<b>0.8</b>	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	<b>0.7</b>	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	<b>0.6</b>	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	<b>0.5</b>	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
<b>0.4</b>	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26	

Note: VIH/L(ac) = +/-TBDmV, VIH/L(dc) = +/-TBDmV; relative to VREFCA.

## 17 General reliability parameters

Table 76 - General reliability parameters

Parameters	Value	Notice
ESD level/volt	HBM: 2kV CDM: 500V	
ILU	>100mA, 1.5*Vddmax	
MSL	3	
Reliability Grade	NA	
Number of Machine On/Off Cycles	TBD	
Maximum PCB assembly reflows	3	
Machine Life (kPOH)	TBD	
LifeTime	10years	
	0.248g	
Maximum Allowable External Environment Temperature Change Rate For Normal Operation (EETCR <sub>Max</sub> )	15°C/Min	

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## 18 FAQ

### 18.1 Suggestions on Chip Mixing Scenarios

It is not recommended that the chip be used together with chips from other vendors. Because the I/O features of chips from different vendors vary greatly, SI/PI issues may occur, affecting board reliability.

### 18.2 Description of Voltage Steps During VDD&VDDQ Power-on

During the power-on process, the VDD and VDDQ transiently require large currents. If the power supply capability of the board-level is weak or the board-level PI assessment is incomplete, a platform voltage may occur during the power-on process. You need to perform a complete PI analysis on the power supply during board-level design to avoid PI problems. The power supply capability of the PSU must meet the requirement of 180 mA@400 ns.

### 18.3 VrefDQ Setup Procedure Requirements

Refer to chapter 《DQ Vref Training》 of the standard protocol of DDR4.

VREF needs to be configured in three steps according to the protocol requirements. If the VREF is configured in one step, errors may occur.

Description of the three-step process (AX indicates the bit corresponding to MR6):

- 1) A7 and A6 are configured at the same time.
- 2) A5:A0, Set the value of Vref-DQ in step 2.
- 3) A7=0

### 18.4 Considerations for the use of the s/hPPR feature

The product Only support Fail Row Address repair(PPR) feature in X16 mode, Even you can get MPR info(MPR0[7:6]=0b11) from X8 product .

Here are some Considerations for the use of the s/hPPR feature:

- 1) At the step three Gurdkey configuraton, A6:A0 must be 0b1111111.
- 2) At the step six, after WL, PPR is considered to be successful if either of the last two beats of DQ0 is low.
- 3) At the step six, when the Parity function is enabled, the refresh command cannot be directly sent for the next cycle of precharge. (The protocol sequence diagram indicates that the refresh instruction can be sent in the next beat.) Refresh is sent after the interval of tRP.
- 4) sPPR associated row address as below.

**Table 77 –sPPR associated row address**

sPPR Associated Row Addresses						
BA1	BA0	A17	A16	A15	A14	A0

### 18.5 Precautions for Using the s/hPPR Feature

When the h/sPPR action is executed, if the corresponding line is repaired by the CP/FT test, row access conflict occurs in the granularity, resulting in multi-row failure in an uncertain range. (Probability less than  $128 / 16384 = 0.78\%$ ).

If the s/hPPR specifications still need to be restricted on the product board, refer to the following suggestions.

Item	Specification Category	Application Suggestions and Instructions
1	hPPR	After the PPR repair is performed, the Chipsets are tested using a simple full-space scanning algorithm, and if the test passes, the repair is successful. The system enters the

		<p>normal application state.</p> <p>You can use sPPR to fix the faulty address first, and then use hPPR to fix the address after the full space test is passed. If the test fails, the hPPR process is disabled. In this way, the opportunity to roll back the PPR repair is retained, ensuring that the final hPPR repair is performed without introducing fault address expansion.</p>
2	sPPR	<p>It is the same as the preceding hPPR specifications. After the fault is rectified, perform a full-space test to check whether the fault is rectified successfully. If the fault fails to be rectified, an alarm is generated at the software layer or a reset is performed to roll back the fault.</p> <p>Due to the requirement of full-space test, the function of saving non-related line data of granularities cannot be implemented when the sPPR process is implemented.</p>

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